Hardware Modeling [VU] (191.011)
– WS25 –
Synchronizers and Debouncers

Florian Huemer & Sebastian Wiedemann & Dylan Baumann

WS 2025/26

Modified: 2025-12-16, 16:05 (f8a58e9)

Recall: MTBU Estimation

- We can get a statistical estimate of the MTBU

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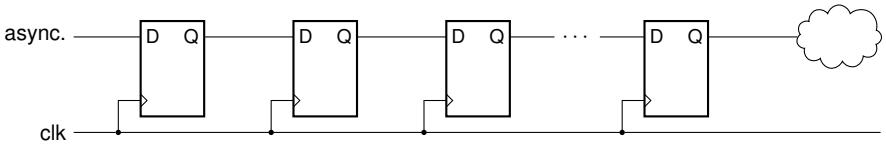
  - Increasing t_{res} is a mechanism to increase the MTBU
  - However: MTBU can never become infinite!
- Harnessed by *synchronizers*
  - Trade-off performance for a higher MTBU

Waiting Synchronizers

- Chain of flip-flops



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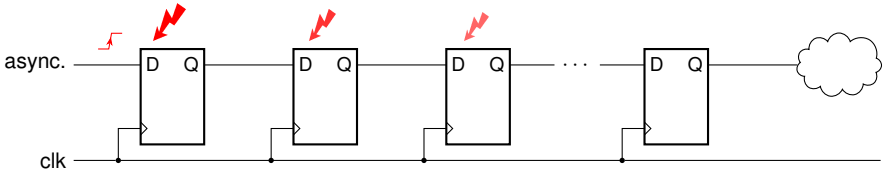

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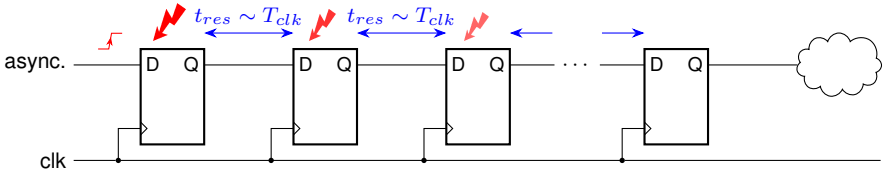

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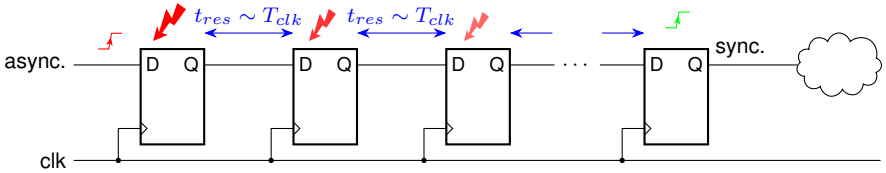

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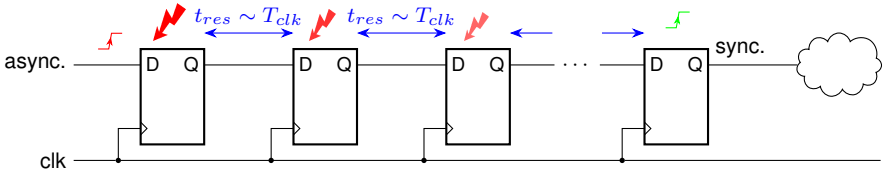

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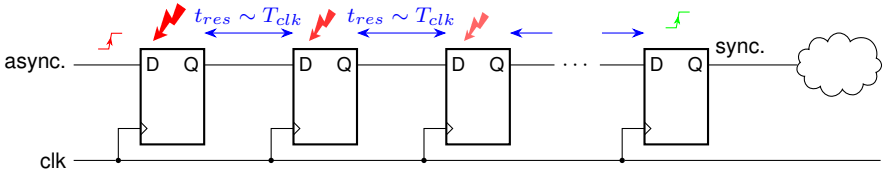

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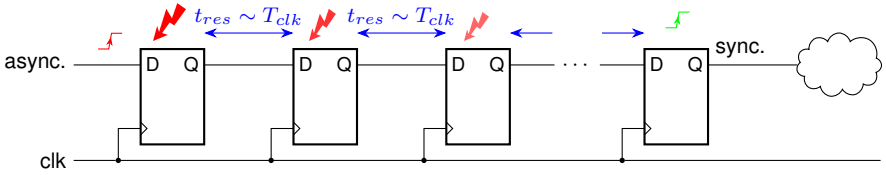
  $\Rightarrow$ Exponential increase in MTBU **per** flip-flop
- In practice often two flip-flops, three to be on the safe side
  - Trade-off between latency and MTBU



VHDL Implementation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1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity synchronizer is
5    generic (
6      STAGES  : natural;
7      RES_VAL : std_ulogic
8    );
9    port (
10     clk   : in std_ulogic;
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architecture arch of synchronizer is
  signal ffs: std_ulogic_vector(0 to STAGES);
begin
  process (clk, res_n) begin
    if res_n = '0' then
      ffs <= (others => RES_VAL);
    elsif rising_edge(clk) then
      ffs(0) <= async;
      for i in 1 to STAGES loop
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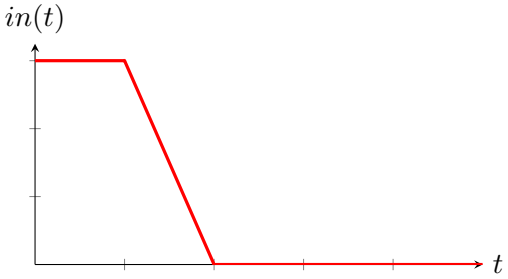
  - A synchronizer does **not** prevent metastability!
- A single flip-flop alone is not a synchronizer
- The MTBU is a statistical quantity
  - No guarantee for upset-freedom at any time

Bouncing Inputs

- Asynchronous inputs are not the only problem at interfaces



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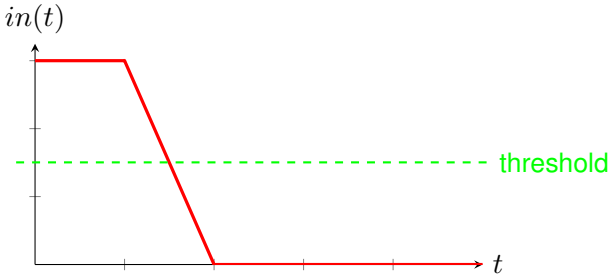

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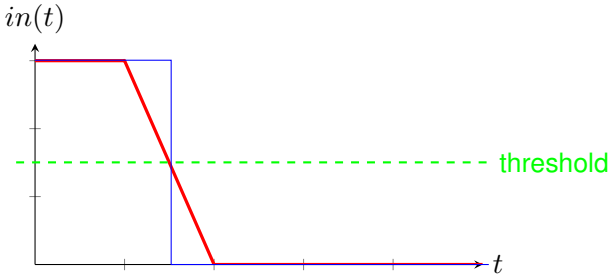

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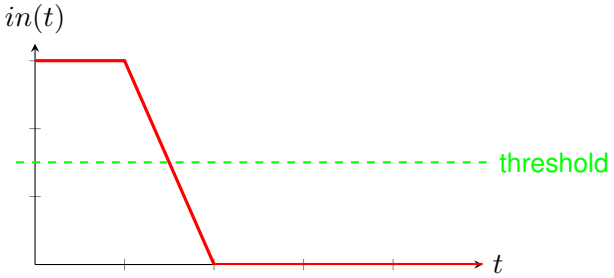

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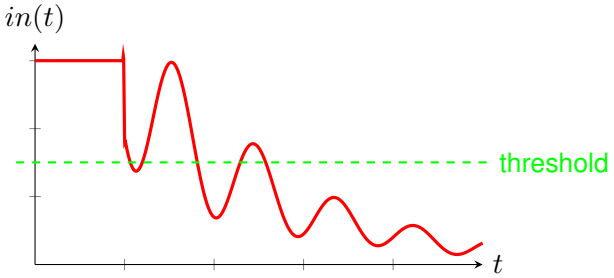

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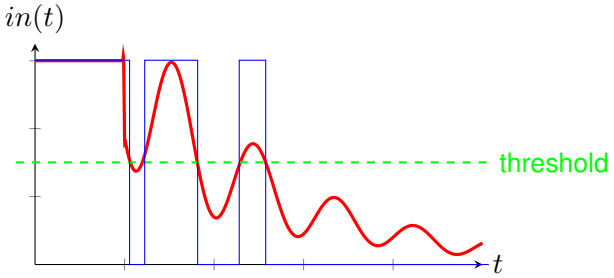

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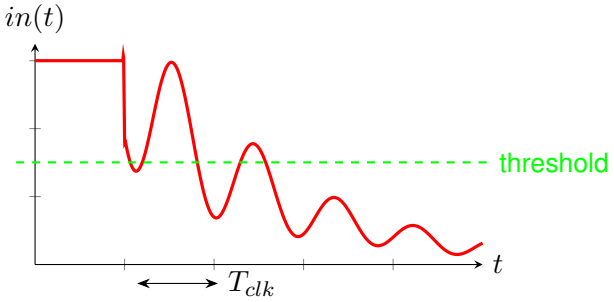

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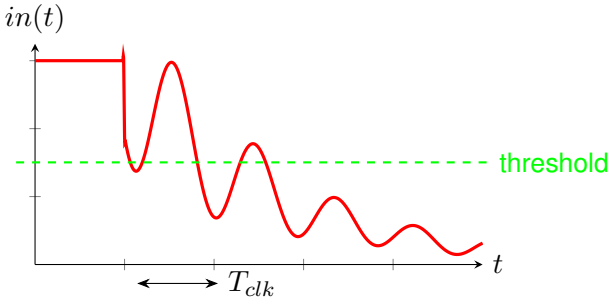
  - Depending on clock frequency, takes multiple (hundred) clock cycles
- May upset input FFs or leads to unwanted transitions



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  - Software-based debouncing

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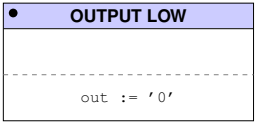

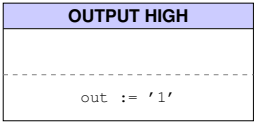

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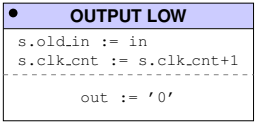

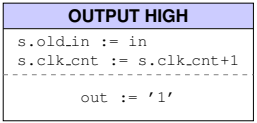

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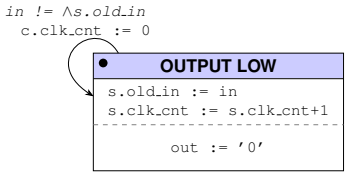

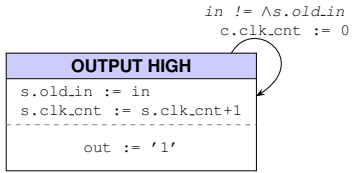

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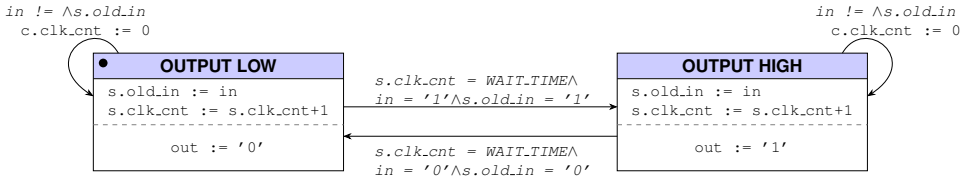

Lecture Complete!