Hardware Modeling [VU] (191.011)
– WS25 –
Synchronizers and Debouncers

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Recall: MTBU Estimation

- We can get a statistical estimate of the MTBU

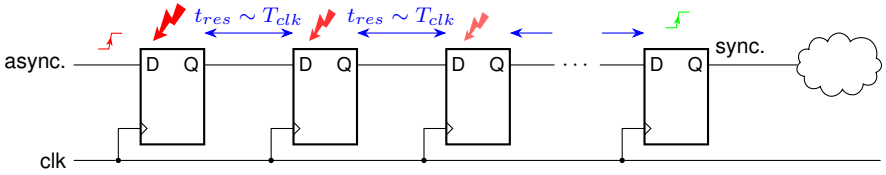
$$MTBU = \frac{1}{\lambda_{in} \cdot f_{clk} \cdot T_W} \cdot e^{\frac{t_{res}}{\tau_C}}$$

- Exponential dependence of MTBU on time to resolve t_{res}
  - Increasing t_{res} is a mechanism to increase the MTBU
  - However: MTBU can never become infinite!
- Harnessed by *synchronizers*
  - Trade-off performance for a higher MTBU

Waiting Synchronizers

- Chain of flip-flops
  - Pass metastable output to next flip-flop in chain
  - No comb. logic between flip-flops $\Rightarrow$ majority of clock period for resolution
  - Asynchronous input is “synchronized” to the clock
- Overall resolution time is the sum of the individual ones

  $\Rightarrow$ Exponential increase in MTBU **per** flip-flop
- In practice often two flip-flops, three to be on the safe side
  - Trade-off between latency and MTBU



VHDL Implementation


```vhdl
library ieee;
use ieee.std_logic_1164.all;

entity synchronizer is
  generic (
    STAGES  : natural;
    RES_VAL : std_ulogic
  );
  port (
    clk   : in std_ulogic;
    res_n : in std_ulogic;
    async : in std_ulogic;
    sync  : out std_ulogic
  );
end entity;
```

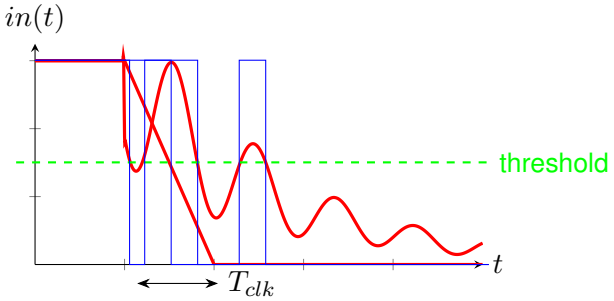
```vhdl
architecture arch of synchronizer is
  signal ffs: std_ulogic_vector(0 to STAGES);
begin
  process (clk, res_n) begin
    if res_n = '0' then
      ffs <= (others => RES_VAL);
    elsif rising_edge(clk) then
      ffs(0) <= async;
      for i in 1 to STAGES loop
        ffs(i) <= ffs(i-1);
      end loop;
    end if;
  end process;
  sync <= ffs(STAGES);
end architecture;
```

Important Aspects

- MTBU can be made *arbitrarily* large by appropriate synchronizer
  - A synchronizer does **not** prevent metastability!
- A single flip-flop alone is not a synchronizer
- The MTBU is a statistical quantity
  - No guarantee for upset-freedom at any time

Bouncing Inputs

- Asynchronous inputs are not the only problem at interfaces
- Some mechanical contacts may “bounce” due to their construction
  - For example: Mechanical buttons, switches
  - Instead of clean transition dampened oscillation
  - Depending on clock frequency, takes multiple (hundred) clock cycles
- May upset input FFs or leads to unwanted transitions

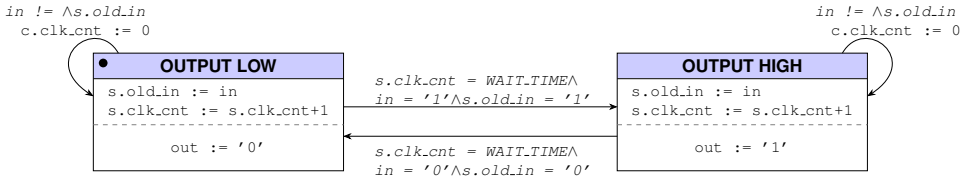


Counter Measures

- Simply filter-out sequence of input transitions that is “too fast”
  - Analog (low pass) filtering
  - Digital filtering to check if output stabilizes
    - Use timer to wait (FSM)
    - Alternatives exist
  - Software-based debouncing

Debouncer Implementation

- Digital debouncing FSM
  - Debouncer either outputs zero or high
  - If the input changes, reset counter to count time since transition
  - When input change is stable, change output



Lecture Complete!