Hardware Modeling [VU] (191.011)
– WS25 –

Synchronous Design Style

Guest Lecture by Prof. Steininger

WS 2025/26

Modified: 2025-12-16, 16:04 (f8a58e9)

Combinational Logic Gates

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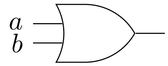

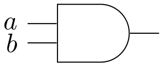

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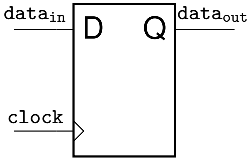

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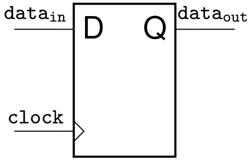

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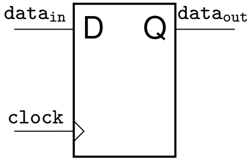

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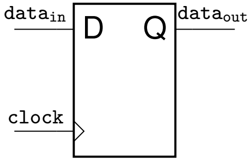

CLK	D	Q_{old}	Q
$\uparrow$	0	0	0
$\uparrow$	0	1	0
$\uparrow$	1	0	1
$\uparrow$	1	1	1
0	X	0	0 (Q_{old})
0	X	1	1 (Q_{old})
1	X	0	0 (Q_{old})
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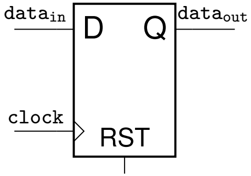
- Optional: (synchronous or asynchronous) reset input (RST)



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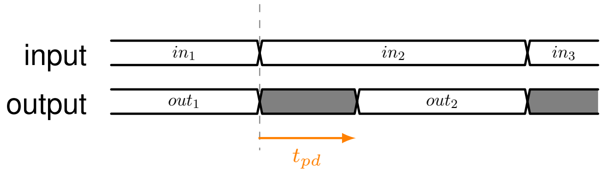

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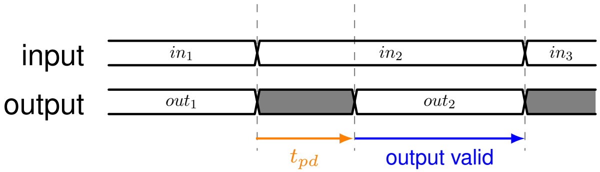

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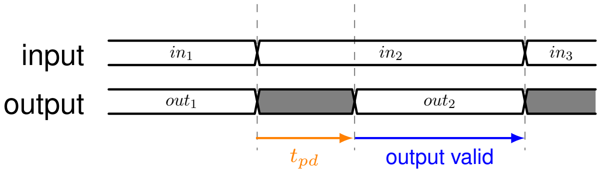

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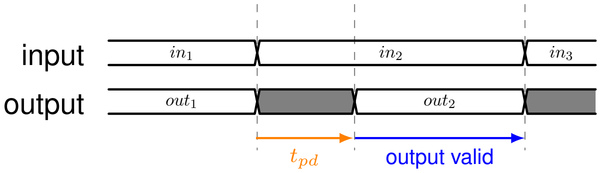

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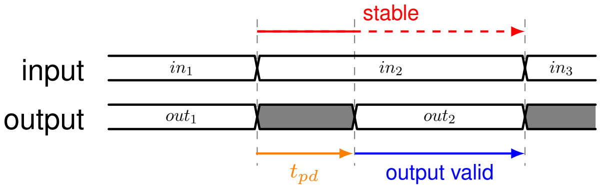
  - After t_{pd} the output remains stable while the input does



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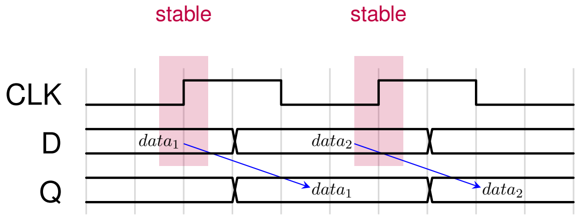

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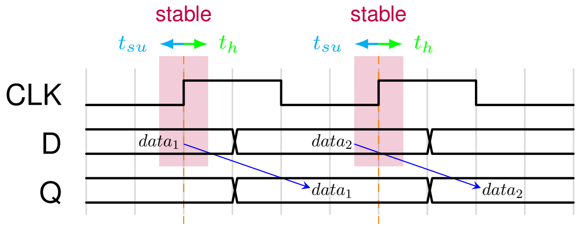

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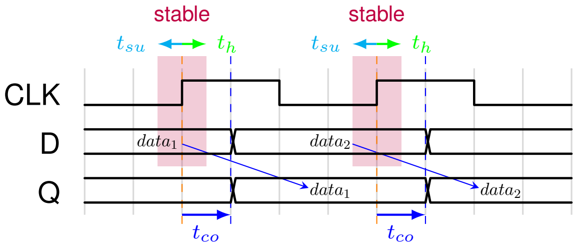
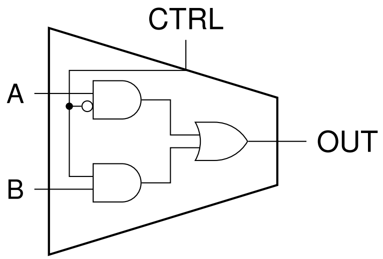
  - Output changed after **clock-to-output** time (t_{co})



Building Functions from Gates

- Larger functions are composed of many simple gates



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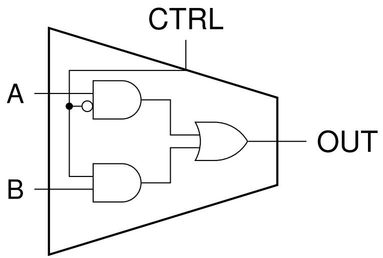

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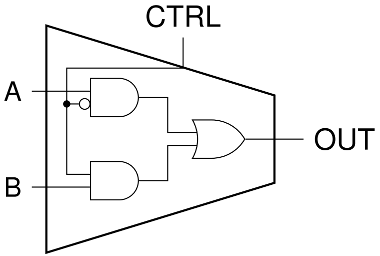

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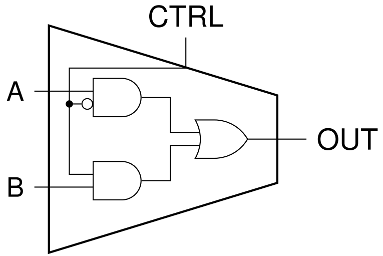

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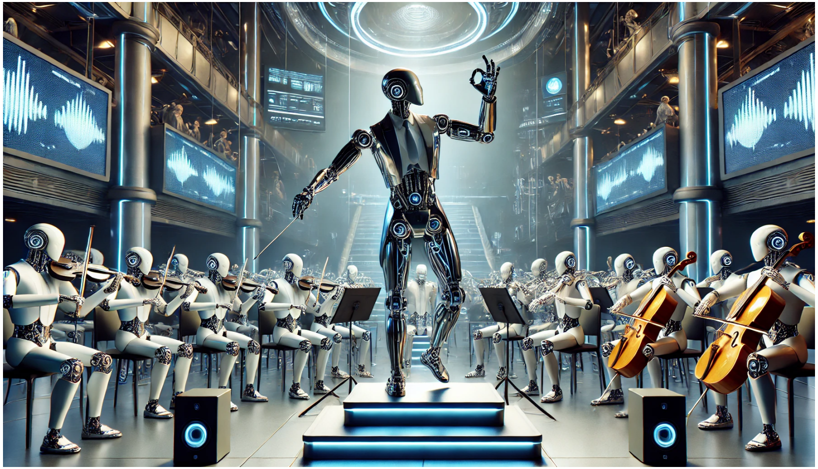
$\Rightarrow$ Requires coordination!

Coordination in Real Life



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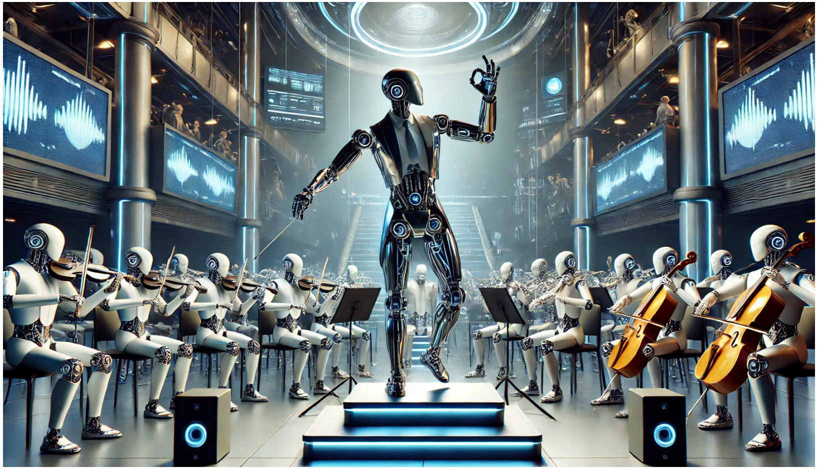

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- A global plan ensures the desired result as a sum of all activities

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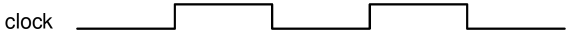

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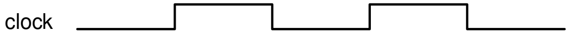

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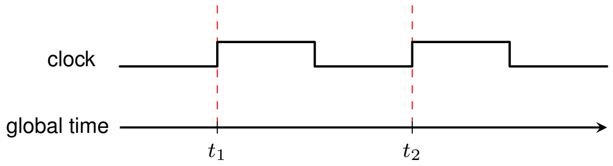

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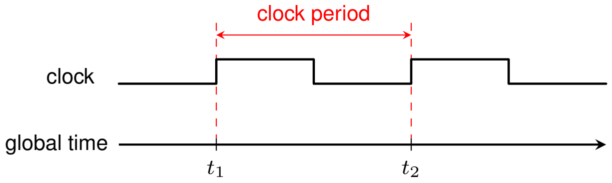

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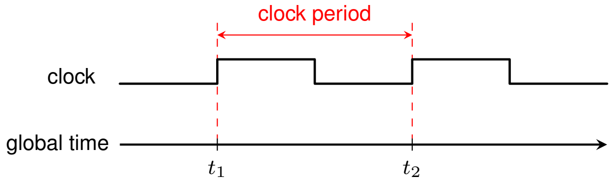

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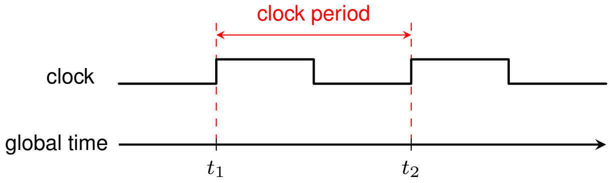

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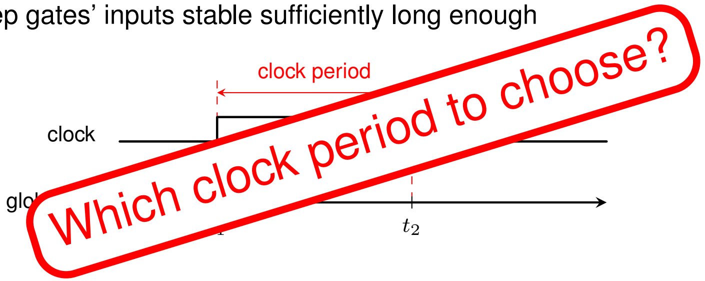

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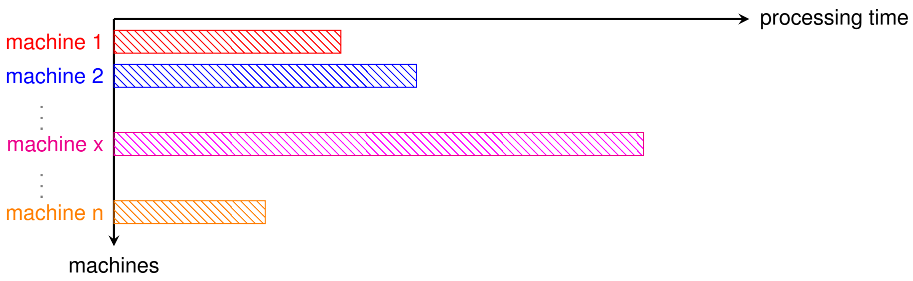

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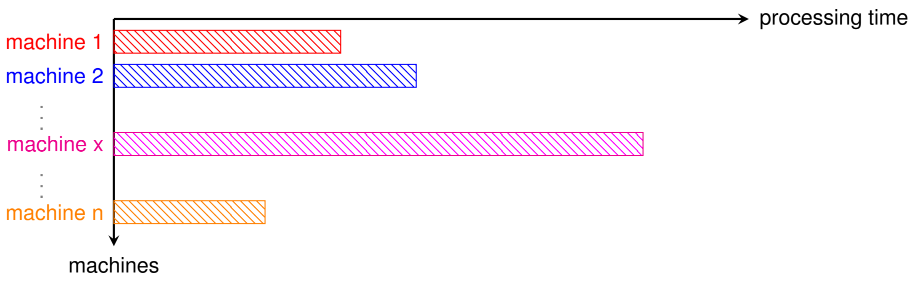

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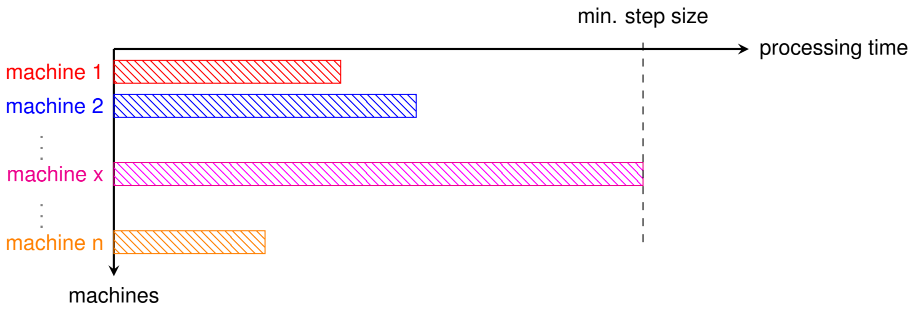
- Max. machine processing time $\Rightarrow$ Min. time step between movements



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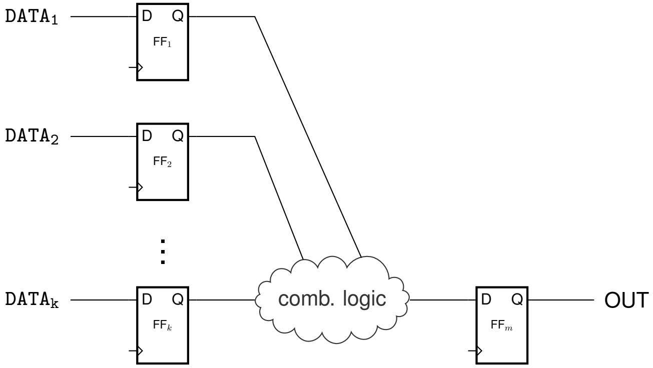
- For the best performance we choose our clock frequency close to the maximum from the STA

Static Timing Analysis Illustration



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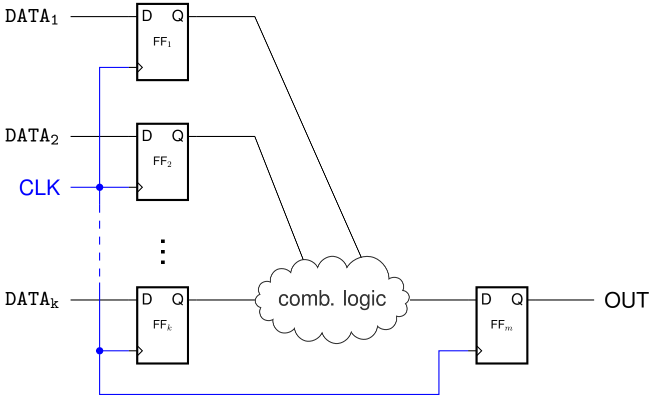

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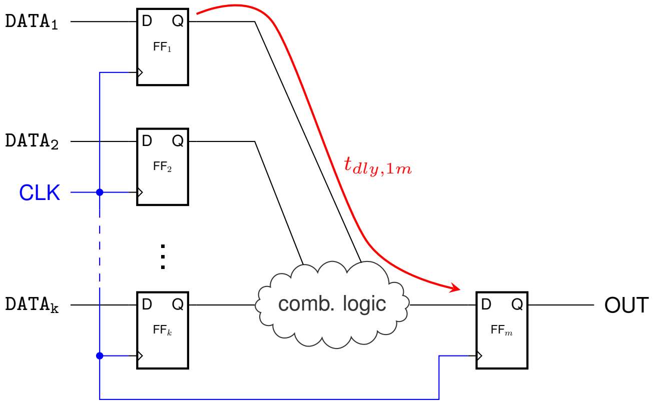

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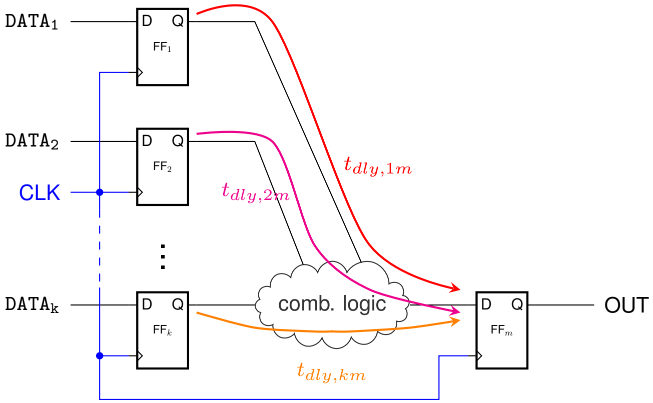
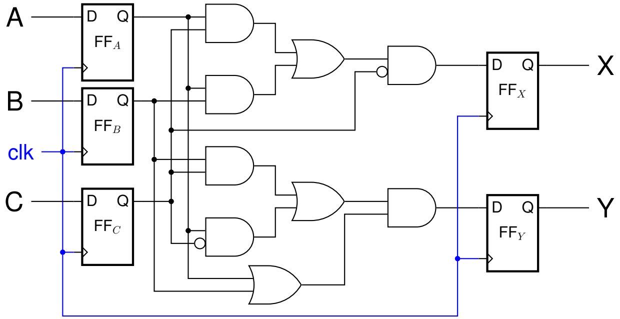


Calculation Example

What is the highest possible clock frequency f_{clk}?



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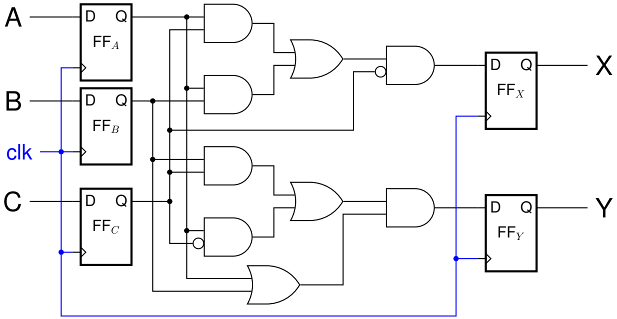

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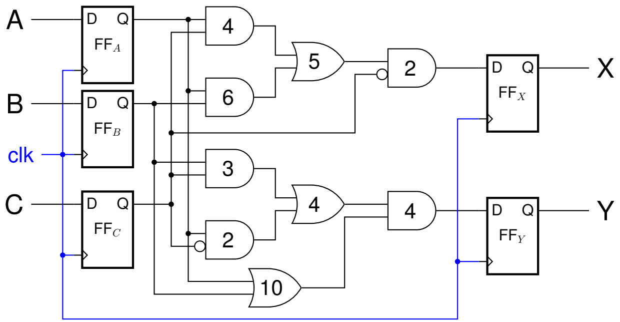

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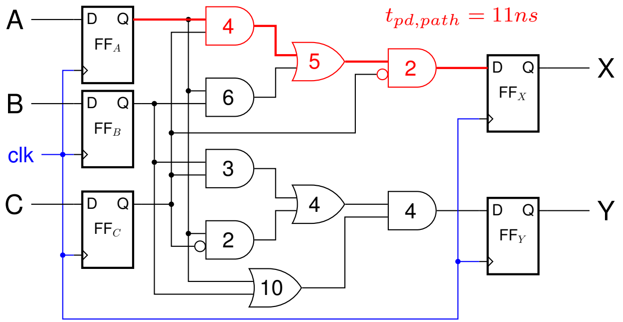

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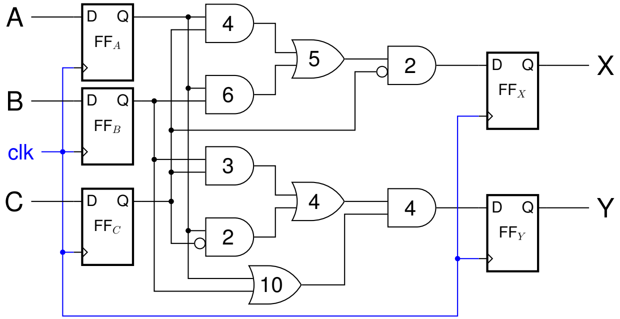

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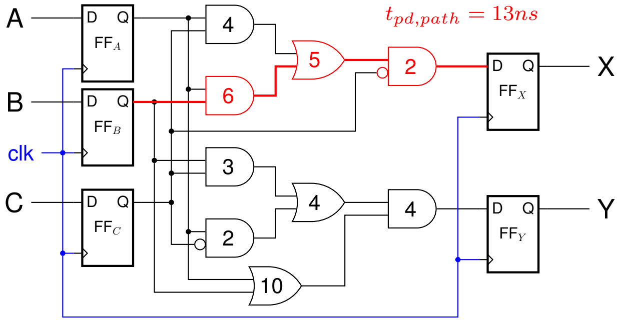

path	delay [ns]
$FF_A \rightarrow FF_X$	11
$FF_A \rightarrow FF_X$	13
$FF_A \rightarrow FF_Y$	10
$FF_A \rightarrow FF_Y$	14
$FF_B \rightarrow FF_X$	13
$FF_B \rightarrow FF_Y$	11
$FF_B \rightarrow FF_Y$	14
$FF_C \rightarrow FF_X$	11
$FF_C \rightarrow FF_X$	2
$FF_C \rightarrow FF_Y$	11
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Calculation Example

What is the highest possible clock frequency f_{clk}?
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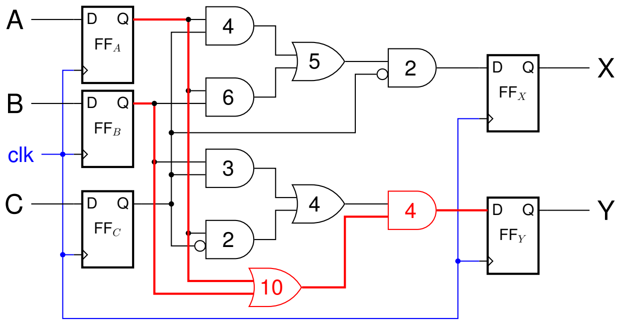

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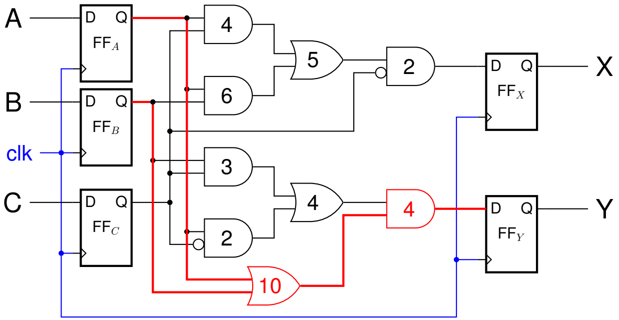
$$T_{clk} = (14 + 1 + 1)ns \Rightarrow f_{clk} = T_{clk}^{-1} = (16ns)^{-1} = 62.5MHz$$



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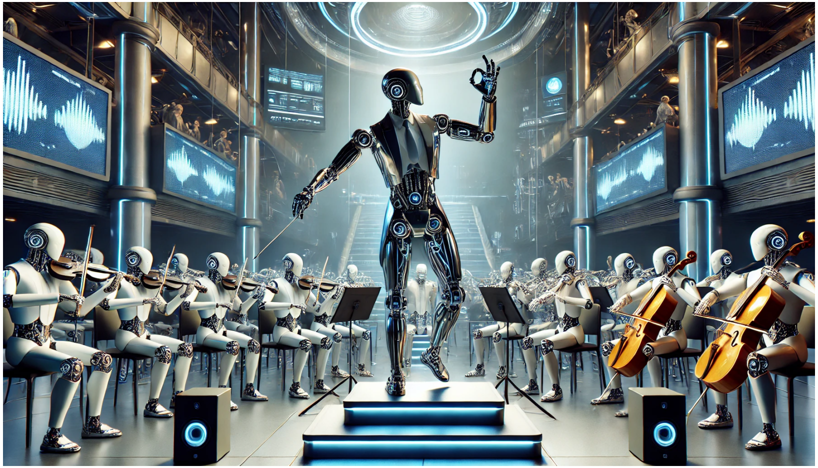
Benefits of Synchronous Design



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- Proven in practice
  - Billion working designs

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- Rigid timing, no graceful degradation
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- However: synchronous design is the most widely used design style
  - Alternatives exist (advanced courses)

Lecture Complete!