Hardware Modeling [VU] (191.011)
– WS25 –
Structural Modeling

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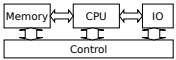
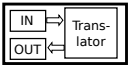
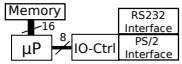
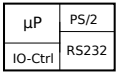
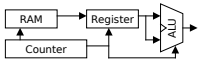
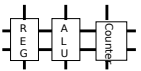
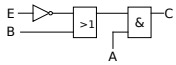
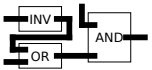
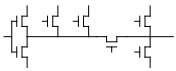
Modified: 2025-12-16, 16:10 (f8a58e9)

Introduction

	Behavior	Structure	Geometry
System Level	Inputs : Keyboard Output: Display Function:		
Algorithmic Level	while input read English text translate to German output German Text		

Register Transfer Level (RTL)	if A=`1` then
	B:= B+1
	else
	B:= B
	end if
			

Logic Level	D = NOT E C = (D OR B) AND A		
Circuit Level	$\frac{dU}{dt} = R\frac{dI}{dt} + \frac{I}{C} + L\frac{d^2I}{dt^2}$		

Introduction (cont'd)

Structual Modeling

Create complex modules by combining and interconnecting (simpler) sub-modules.

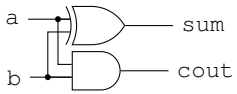
Top-Level Design/Entity

The design unit (entity) that sits on highest layer of a hierarchical hardware design.

Unit Under Test (UUT)

The module instantiated in a testbench and whose behavior is verified.

Creating Instances – Example: Half Adder

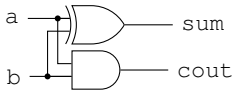



```vhdl
entity xor_gate is
 port (
  a, b : in std_ulogic;
  x : out std_ulogic
 );
end entity;

architecture arch of xor_gate is
begin
 x <= a xor b;
end architecture;
```

```vhdl
entity and_gate is
 port (
  a, b : in std_ulogic;
  x : out std_ulogic
 );
end entity;

architecture arch of and_gate is
begin
 x <= a and b;
end architecture;
```

Creating Instances – Example: Half Adder


```
1  entity ha is
2   port (
3    a, b : in std_ulogic;
4    sum, cout : out std_ulogic
5   );
6  end entity;
7
8  architecture arch of ha is
9  begin
10  and_gate_inst : entity work.and_gate
11  port map (a, b, cout);
12
13  xor_gate_inst : entity work.xor_gate
14  port map (a, b, sum);
15 end architecture;
```



- Instances → statement part
- Two instantiation statements
- Positional association
- Inputs must be readable, outputs writable

Port Map

- Port map syntax

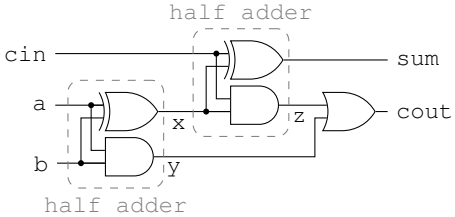
```
port map(association_list)
```

- Part in parentheses → Association list 
- Named and positional associations possible
- **Named association** oftentimes preferable over positional association because of better
  - clarity
  - maintainability
  - flexibility
  - robustness (w.r.t. connection bugs)
- Association list syntax

```
association_list ::= assoc_elem {, assoc_elem}
assoc_elem ::= [formal_part => ]actual_part
```

- Don't mix association styles in port maps

Port Map - Example: Full Adder




```vhdl
entity fa is
 port (
  a, b, cin  : in std_ulogic;
  sum, cout : out std_ulogic
 );
end entity;
```

```vhdl
architecture arch of fa is
 signal x, y, z : std_ulogic;
begin
 ha1 : entity work.ha
 port map(a, b, x, y);

 ha2 : entity work.ha
 port map(
  a => cin,
  b => x,
  cout => z,
  sum => sum
 );

 cout <= y or z;
end architecture;
```

Unused Ports

Unused outputs

- Use `open` keyword
- Don't leave unconnected!

```
1  [...]
2  signal a, b, c, m : std_ulogic;
3 begin
4  majority : entity work.fa
5  port map (
6   a => a,
7   b => b,
8   c => c,
9   sum => open, -- not connected
10  cout => m
11 );
12 [...]
```

Unused inputs

- Connect to constant
- If not connected $\rightarrow$ default value

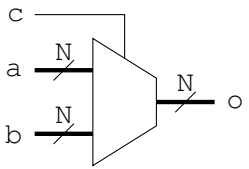
```
1  [...]
2  signal a, b, sum, cout : std_ulogic;
3 begin
4  half_adder : entity work.fa
5  port map (
6   a => a,
7   b => b,
8   c => '0', -- constant
9   sum => sum,
10  cout => cout
11 );
12 [...]
```

Generic Map

- Generic map syntax
  `generic map(association_list)`
- Must appear before port map
- Use named association and avoid the positional style
- Formal parts must be compile-time constants (generics cannot be connected to signals)

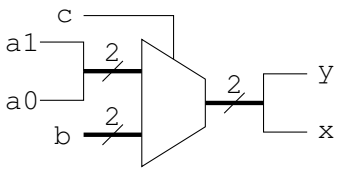
Generic Map – Example: Multiplexer


```
1  entity mux is
2   generic (
3    N : positive
4   );
5   port (
6    c : in std_ulogic;
7    a : in std_ulogic_vector(N-1 downto 0);
8    b : in std_ulogic_vector(N-1 downto 0);
9    o : out std_ulogic_vector(N-1 downto 0)
10  );
11 end entity;
12
13 architecture arch of mux is
14 begin
15  o <= a when c = '0' else b;
16 end architecture;
```



Generic Map – Example: Multiplexer (cont'd)


```
1  [...]
2  signal c : std_ulogic;
3  signal a0, a1 : std_ulogic;
4  signal b : std_ulogic_vector(1 downto 0);
5  signal x, y : std_ulogic;
6 begin
7  mux_inst : entity work.mux
8  generic map (N => 2)
9  port map (
10   c => c,
11   a => a1 & a0,
12   b => b,
13   o(0) => x,
14   o(1) => y
15  );
16  [...]
```



Components

- Components are *“entity prototype”*
- Component declaration syntax

```
component NAME is
[ generic ( {generic_element;} generic_element ); ]
[ port ( {port_element;} port_element ); ]
end component;
```

- Components can be put in
  - packages
  - declarative part of architectures (blocks and generate statements)

Components (cont'd)

- Instantiation example
  - Entity: `i : entity work.fa port map (...);`
  - Component: `i : fa port map (...);`
  - Component (explicit): `i : component fa port map (...);`
- Modularity, abstraction and separation of concerns
- Compilation order
- Entity may not always be available
- Mixed-language designs

Architecture Selection

- Multiple different architectures possible for a single entity
  $\Rightarrow$ How to select one?
- Two possibilities
  - Specify architecture, when an **entity** is instantiated
    Caution: This does not work for components!
  - Configurations

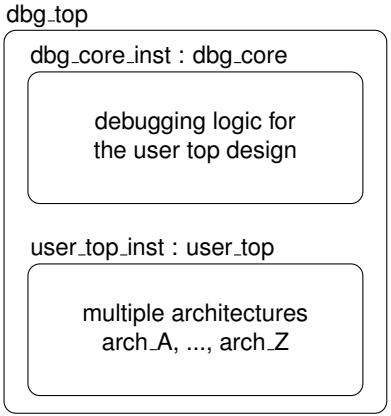
Entity Instantiations


```
1  entity mystery is
2   port (
3    a, b : in std_ulogic;
4    x : out std_ulogic
5   );
6  end entity;
7
8  architecture a1 of mystery is
9  begin
10  x <= a and b;
11 end architecture;
12
13 architecture a2 of mystery is
14 begin
15  x <= a xor b;
16 end architecture;
```

```
1  entity ha is
2   port (
3    a, b : in std_ulogic;
4    sum, cout : out std_ulogic
5   );
6  end entity;
7
8  architecture arch of ha is
9  begin
10  and_gate : entity work.mystery(a1)
11  port map (a, b, cout);
12
13  xor_gate : entity work.mystery(a2)
14  port map (a, b, sum);
15 end architecture;
```

Configurations


```
1 configuration dbg_top_conf of dbg_top is
2  for dbg_top_arch
3   for user_top_inst : user_top
4    use entity user_top(arch_A);
5   end for;
6  end for;
7 end configuration;
```



Lecture Complete!