Hardware Modeling [VU] (191.011)
– WS25 –
Sequential Circuit Elements in VHDL

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WS 2025/26

Modified: 2025-12-16, 16:04 (f8a58e9)

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  - Flip-flops: JK, T, **D**
- Relevant for this course: Data (D) type

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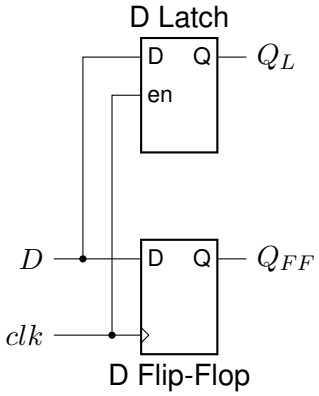
Register

Registers are collections of D flip-flops (latches) that hold data that logically belong together.

D Latches vs. D Flip-Flop



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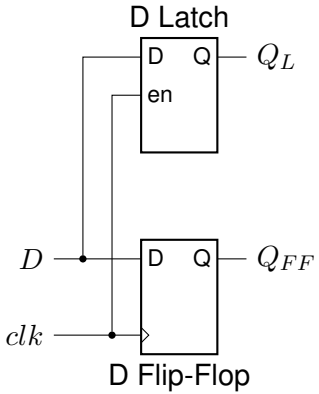

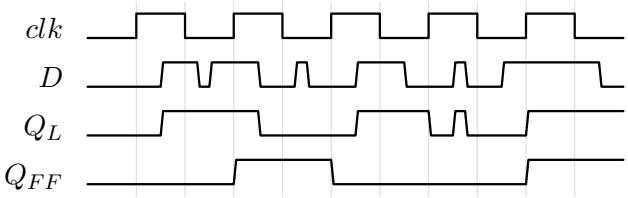

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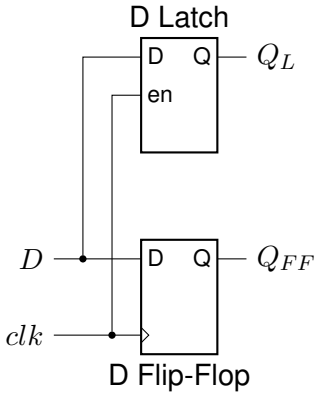

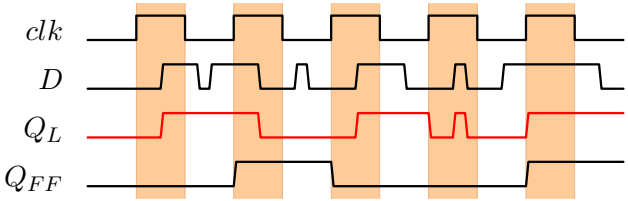

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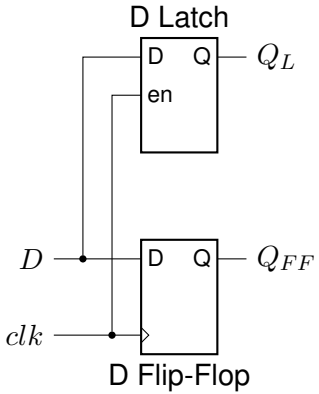

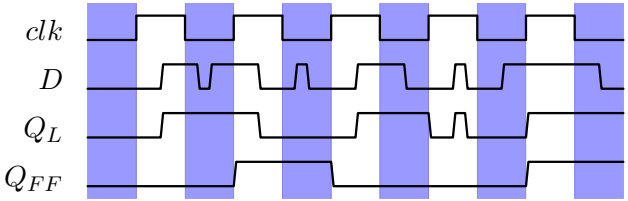

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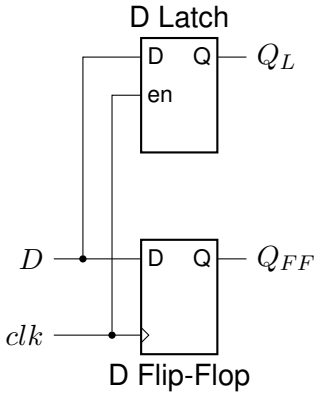

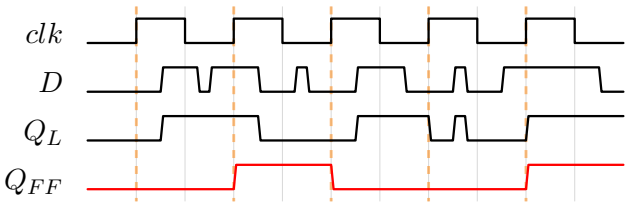

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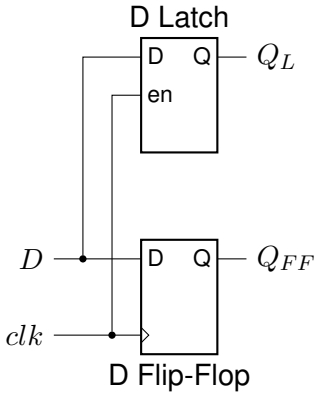

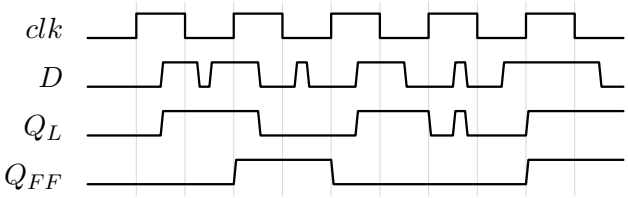

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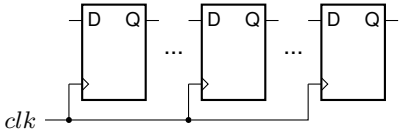

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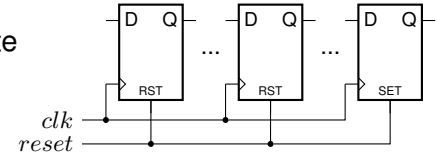

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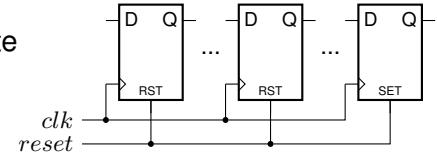

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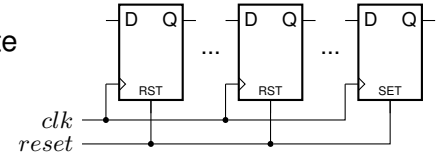

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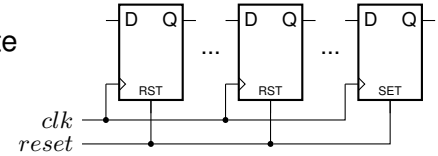

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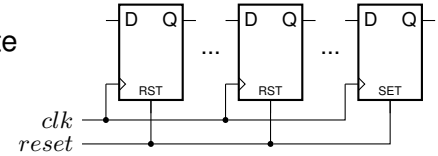

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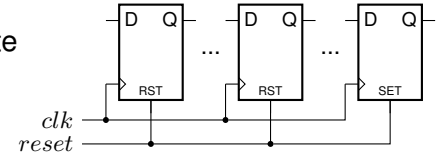

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- Typical reset value is zero/low (sometimes different values are necessary)
- Testbenches must **always** activate the UUT's reset upon startup

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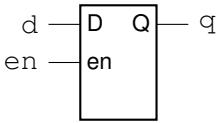


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  port (
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end entity;

architecture arch of dlatch is
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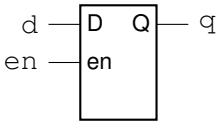


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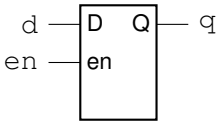


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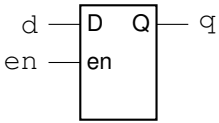

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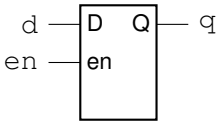

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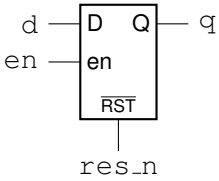


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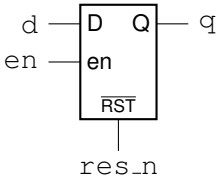


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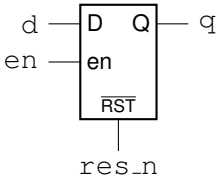


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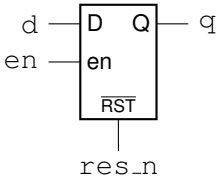


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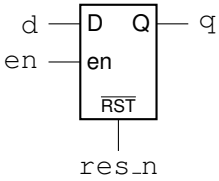

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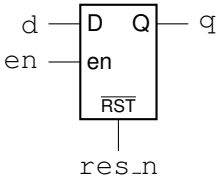

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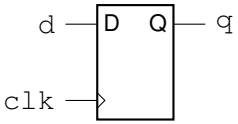
D Flip-Flop




```
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2 entity dff is
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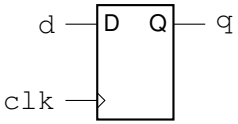


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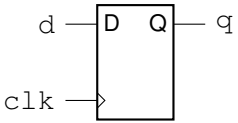


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Problem

How can we detect the event of a signal transition?

D Flip-Flop

- Helper function

```
1 function rising_edge(signal s : std_ulogic) return boolean is
2 begin
3   return [...];
4 end function;
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9  architecture arch of dff is
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```
s'event and s = '1'
```

- What if `clk` changes from, e.g., `'U'` to `'1'`?

Signal Edges – `last_value` Attribute

- VHDL standard

> "*For a signal* `s`*, if an event has occurred on* `s` *in any simulation cycle,* `s'last_value` *returns the value of* `s` *prior to the update of* `s` *in the last simulation cycle in which an event occurred; otherwise,* `s'last_value` *returns the current value of* `s`."

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- Improved edge detection expression

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- What if `clk` changes from `'L'` to `'H'`?

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  - `'U','X','Z','W','-'` → `'X'`
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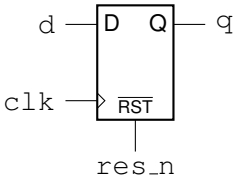
- `rising/falling_edge` as defined in `std_logic_1164` package
- The `standard` package defines `rising/falling_edge` for the types
  - `bit`
  - `boolean`

Reset




```
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2   port (
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8 end entity;
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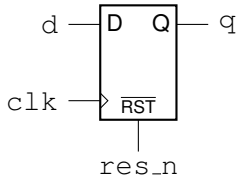
Reset

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Reset Condition

When is the reset evaluated?

Reset (Cont'd)

Synchronous Reset

Asynchronous Reset

Reset (Cont'd)

Synchronous Reset

- Reset signal is only evaluated at the active clock edge

```
 9 architecture sync of dff_r is
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- Reset signal is level-sensitive

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- `res_n` **not** in sensitivity list

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Enable Input

- What if a flip-flop should not be updated each clock cycle?

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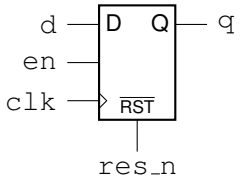
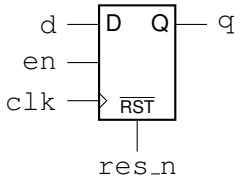
  - $\Rightarrow$ Use a dedicated enable signal




```
1 entity dff_en is
2   port (
3     clk   : in  std_ulogic;
4     res_n : in  std_ulogic;
5     en    : in  std_ulogic;
6     d     : in  std_ulogic;
7     q     : out std_ulogic
8   );
```

Enable Input

- What if a flip-flop should not be updated each clock cycle?
  - $\Rightarrow$ Use a dedicated enable signal




```
11  process(clk, res_n)
12  begin
13    if res_n = '0' then
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15    elsif rising_edge(clk) then
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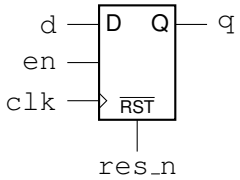


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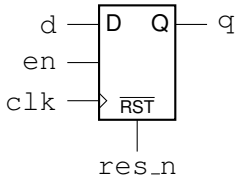
- Structure matters!
  - **Always** use the patterns shown in this lecture

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- What if a flip-flop should not be updated each clock cycle?
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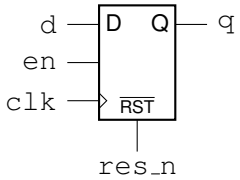
- Structure matters!
  - **Always** use the patterns shown in this lecture
  - Synthesis tools expect certain structures

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Lecture Complete!