Hardware Modeling [VU] (191.011)
– WS25 –
RAM in VHDL (for FPGAs)

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  - Large look-up tables
  - Program and data memory for processors to store instructions and data

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  - Simple dual-port RAM: one read and one write port
  - True dual-port RAM: two read/write ports

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- Memory in modern FPGAs is (almost) always synchronous
  - Read and write operations only happen at a clock edge
  - Some older FPGAs support asynchronous memory

Intel FPGAs

Table 3. Embedded Memory Blocks in Intel FPGA Devices

Device Family	Memory Block Type					
	MLAB (640 bits)	M9K (9 Kbits)	M144K (144 Kbits)	M10K (10 Kbits)	M20K (20 Kbits)	Logic Cell (LC)
Arria® II GX	Yes	Yes	–	–	–	Yes
Arria II GZ	Yes	Yes	Yes	–	–	Yes
Arria V	Yes	–	–	Yes	–	Yes
Intel Arria 10	Yes	–	–	–	Yes	Yes
Cyclone® IV	–	Yes	–	–	–	Yes
Cyclone V	Yes	–	–	Yes	–	Yes
Intel Cyclone 10 LP	–	Yes	–	–	–	Yes
Intel Cyclone 10 GX	Yes	–	–	–	Yes	Yes
MAX® II	–	–	–	–	–	Yes
Intel MAX 10	–	Yes	–	–	–	Yes
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Simple Dual-Port RAM


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1  entity simple_dp_ram is
2   generic (
3    ADDR_WIDTH : positive;
4    DATA_WIDTH : positive
5   );
6   port (
7    clk : in std_ulogic;
8    -- read port
9    rd_en : in std_ulogic;
10   rd_addr : in std_ulogic_vector(ADDR_WIDTH - 1 downto 0);
11   rd_data : out std_ulogic_vector(DATA_WIDTH - 1 downto 0);
12   -- write port
13   wr_en : in std_ulogic;
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Generics to set the data and address width of the memory.

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The clock signal that controls all operations on both the read and the write port.

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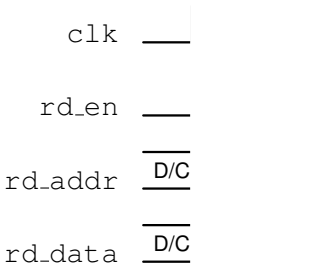
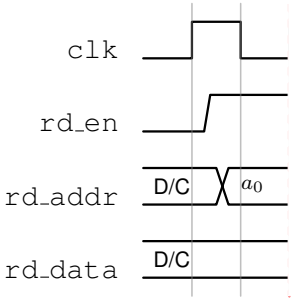
Memory write port.

Read Access



Read Access



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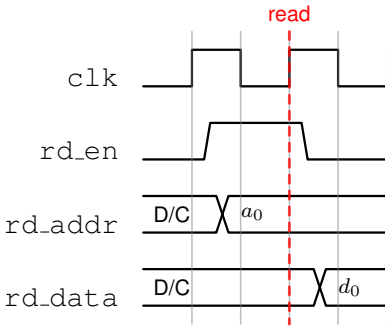

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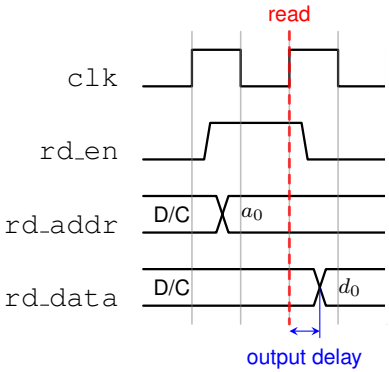

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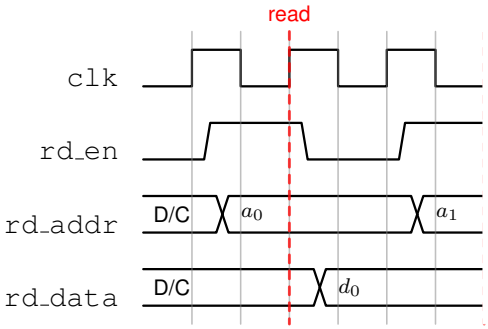

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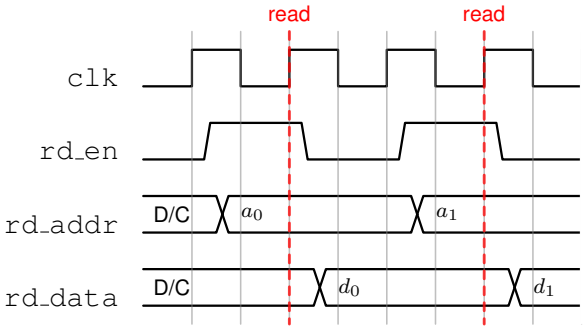

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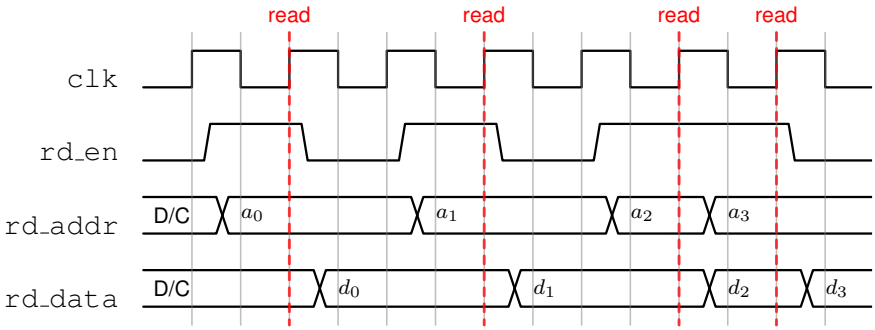
read
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clk
rd_en
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D/C
a_0
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a_3
rd_data
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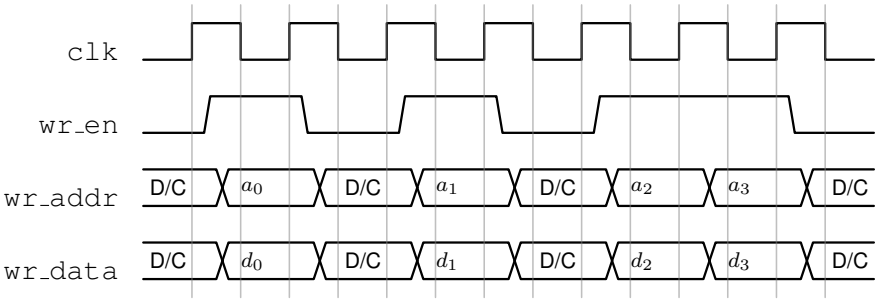
Write Access



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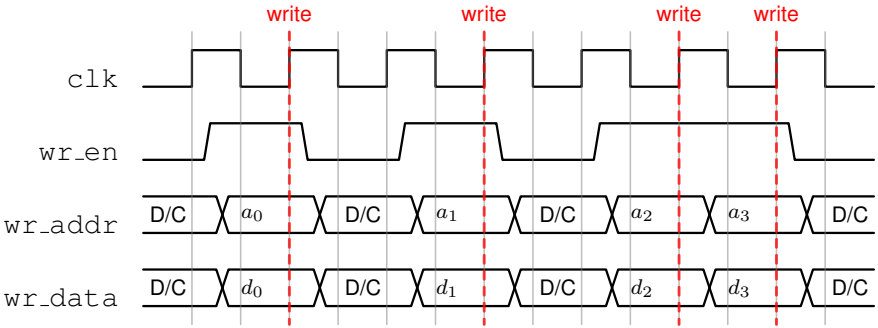

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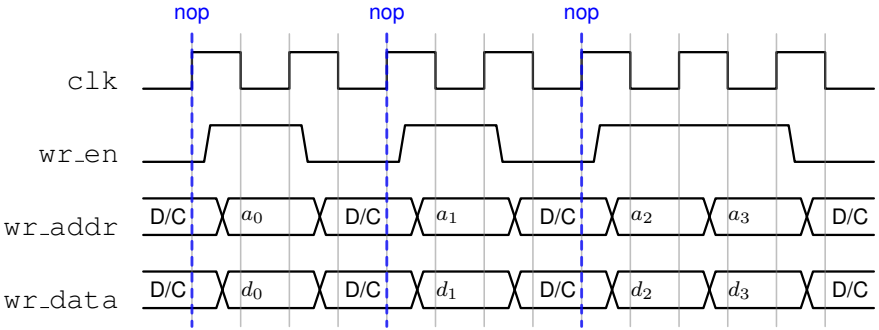

True Dual-Port RAM


```
1  entity true_dp_ram is
2   generic (
3    ADDR_WIDTH : positive;
4    DATA_WIDTH : positive
5   );
6   port (
7    clk : in std_ulogic;
8    -- read/write port 0
9    rw0_rd_en : in std_ulogic;
10   rw0_wr_en : in std_ulogic;
11   rw0_addr : in std_ulogic_vector(ADDR_WIDTH - 1 downto 0);
12   rw0_wr_data : out std_ulogic_vector(DATA_WIDTH - 1 downto 0);
13   rw0_rd_data : out std_ulogic_vector(DATA_WIDTH - 1 downto 0);
14   -- read/write port 1
15   rw1_rd_en : in std_ulogic;
16   rw1_wr_en : in std_ulogic;
17   rw1_addr : in std_ulogic_vector(ADDR_WIDTH - 1 downto 0);
18   rw1_wr_data : out std_ulogic_vector(DATA_WIDTH - 1 downto 0);
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First read/write memory port.

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- Usually supported by FPGA block RAM
- Simultaneous read and write to the same location must be handled carefully
- $\Rightarrow$ dual-clocked/bisynchronous FIFOs

Dual-Clocked RAM - Example


```
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2   generic (
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4    DATA_WIDTH : positive
5   );
6   port (
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8    rd_clk : in std_ulogic;
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RAM Implementation

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Predictability	Deterministic	May cause mismatch in synthesis/simulation tool

Inferred RAM


```
1  architecture beh of simple_dp_ram is
2   subtype ram_entry_t is std_ulogic_vector(DATA_WIDTH - 1 downto 0);
3   type ram_t is array(0 to (2 ** ADDR_WIDTH) - 1) of ram_entry_t;
4   signal ram : ram_t := (others => (others => '0'));
5  begin
6   process(clk)
7   begin
8    if rising_edge(clk) then
9     if wr_en = '1' then
10     ram(to_integer(unsigned(wr_addr))) <= wr_data;
11    end if;
12    if rd_en = '1' then
13     rd_data <= ram(to_integer(unsigned(rd_addr)));
14    end if;
15   end if;
16  end process;
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Type definitions and signal declaration for the signal that actually represents the memory array.

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Synchronous process similar to what is used in the description of flip-flops.

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Implementation of the write port.

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```

Implementation of the read port.

Lecture Complete!