

Hardware Modeling [VU] (191.011)

– WS25 –

Numeric Standard Package

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Integer Arithmetic in Hardware

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numeric_std

Motivation

IEEE Package

Types

Operators

Conversion

- When possible use ranged `integer` for synthesizable code

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HWMod
WS25

numeric_std
Motivation
IEEE Package
Types
Operators
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- However: `integer` type has some limitations

Integer Arithmetic in Hardware

HWMod
WS25

numeric_std
Motivation
IEEE Package
Types
Operators
Conversion

- When possible use ranged `integer` for synthesizable code
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 - Only 32 / 64 bits guaranteed by standard (2008 / 2019)

Integer Arithmetic in Hardware

HWMod
WS25

numeric_std
Motivation
IEEE Package
Types
Operators
Conversion

- When possible use ranged `integer` for synthesizable code
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 - Restricted to Boolean 0 and 1 vs. 9-valued logic

Integer Arithmetic in Hardware

HWMod
WS25

numeric_std
Motivation
IEEE Package
Types
Operators
Conversion

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 - Behavior on over-/underflow undefined $\Rightarrow$ wrap-around **or** runtime error 

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HWMod
WS25

numeric_std
Motivation
IEEE Package
Types
Operators
Conversion

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$\Rightarrow$ IEEE `numeric_std` package 

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HWMod
WS25

numeric_std
Motivation
IEEE Package
Types
Operators
Conversion

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$\Rightarrow$ IEEE `numeric_std` package 

- Requires import from the `ieee` library

```
library ieee;  
use ieee.numeric_std.all;
```

The IEEE numeric_std Package

331

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numeric_std

Motivation

IEEE Package

Types

Operators

Conversion

- `unsigned` and `signed` with respective operator definitions

- `unsigned` and `signed` with respective operator definitions
- Wrap-around on over-/underflow behavior

```
1 process is
2   variable a : integer
3       := integer'high;
4 begin
5   report to_string(a);
6   a := a + 1;
7   report to_string(a);
8   wait;
9 end process;
```

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[...]: 2147483647

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[...]: **error**: overflow detected

```
1 process is
2   variable a : signed(31 downto 0)
3     := to_signed(integer'high, 32);
4 begin
5   report to_string(to_integer(a));
6   a := a + 1;
7   report to_string(to_integer(a));
8   wait;
9 end process;
```

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[...]: 2147483647

[...]: -2147483648

The unsigned and signed Types

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numeric_std

Motivation

IEEE Package

Types

Operators

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- Resolved array types of `std_ulogic`

The unsigned and signed Types

HWMod
WS25

numeric_std

Motivation

IEEE Package

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- Resolved array types of `std_ulogic`
 - Can be interpreted as `std_logic_vector` for arithmetic

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HWMod
WS25

numeric_std

Motivation

IEEE Package

Types

Operators

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- Resolved array types of `std_ulogic`
 - Can be interpreted as `std_logic_vector` for arithmetic
 - Represent unsigned / two's complement binary integers

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HWMod
WS25

numeric_std

Motivation

IEEE Package

Types

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 - Can be interpreted as `std_logic_vector` for arithmetic
 - Represent unsigned / two's complement binary integers

■ Examples

```
signal a : unsigned(3 downto 0) := "1111"; -- 15
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HWMod
WS25

numeric_std

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IEEE Package

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signal a : unsigned(3 downto 0) := "1111"; -- 15
signal b : signed(3 downto 0) := "1111"; -- -1
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HWMod
WS25

numeric_std

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IEEE Package

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- Resolved array types of `std_ulogic`
 - Can be interpreted as `std_logic_vector` for arithmetic
 - Represent unsigned / two's complement binary integers
 - Bit string literal initialization possible

■ Examples

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HWMod
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numeric_std

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IEEE Package

Types

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- Resolved array types of `std_ulogic`
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 - Represent unsigned / two's complement binary integers
 - Bit string literal initialization possible
 - Elements are nine-valued $\Rightarrow$ useful for debugging

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HWMod
WS25

numeric_std

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IEEE Package

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Operators

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- Resolved array types of `std_ulogic`
 - Can be interpreted as `std_logic_vector` for arithmetic
 - Represent unsigned / two's complement binary integers
 - Bit string literal initialization possible
 - Elements are nine-valued $\Rightarrow$ useful for debugging
- Wrap around on over- / underflow $\Rightarrow$ behavior of “real” hardware
- Examples

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signal a : unsigned(3 downto 0) := "1111"; -- 15
signal b : signed(3 downto 0) := "1111"; -- -1
```

Arithmetic Operators

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numeric_std

Motivation

IEEE Package

Types

Operators

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- Most common operators are defined and implemented 

Arithmetic Operators

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WS25

numeric_std

Motivation

IEEE Package

Types

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- Most common operators are defined and implemented 
- Arithmetic: `+`, `-`, `*`, `/`, `rem`, `mod`, `abs`

Arithmetic Operators

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IEEE Package

Types

Operators

Conversion

- Most common operators are defined and implemented 
- Arithmetic: `+`, `-`, `*`, `/`, `rem`, `mod`, `abs`
- Relational: `>`, `<`, `<=`, `>=`, `=`, `/=`
- Logical: Same as for `std_ulogic_vector`
- Shift / rotate: `sll`, `srl`, `rol`, `ror`, `sla`, `sra`

Arithmetic Operators

HWMod
WS25

numeric_std

Motivation

IEEE Package

Types

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- Most common operators are defined and implemented 
- Arithmetic: `+`, `-`, `*`, `/`, `rem`, `mod`, `abs`
- Relational: `>`, `<`, `<=`, `>=`, `=`, `/=`
- Logical: Same as for `std_ulogic_vector`
- Shift / rotate: `sll`, `srl`, `rol`, `ror`, `sla`, `sra`
- `resize` function

Arithmetic Operators

HWMod
WS25

numeric_std

Motivation

IEEE Package

Types

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Conversion

- Most common operators are defined and implemented 
 - Arithmetic: `+`, `-`, `*`, `/`, `rem`, `mod`, `abs`
 - Relational: `>`, `<`, `<=`, `>=`, `=`, `/=`
 - Logical: Same as for `std_ulogic_vector`
 - Shift / rotate: `sll`, `srl`, `rol`, `ror`, `sla`, `sra`
 - `resize` function
- Useful overloads for integer / natural operand

Arithmetic Operators (cont'd)

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Motivation

IEEE Package

Types

Operators

Conversion

```
1 process is
2
3
4 begin
5
6
7
8
9
10
11
12
13
14
15
16     wait;
17 end process;
```

Arithmetic Operators (cont'd)

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WS25

numeric_std

Motivation

IEEE Package

Types

Operators

Conversion

```
1 process is
2   variable u : unsigned(3 downto 0) := "1010";
3   variable s : signed(3 downto 0) := "1010";
4 begin
5
6
7
8
9
10
11
12
13
14
15
16   wait;
17 end process;
```

Arithmetic Operators (cont'd)

HWMod
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numeric_std

Motivation

IEEE Package

Types

Operators

Conversion

```
1 process is
2   variable u : unsigned(3 downto 0) := "1010";
3   variable s : signed(3 downto 0) := "1010";
4 begin
5   report to_string(resize(u, 5));
6
7
8
9
10
11
12
13
14
15
16   wait;
17 end process;
```

Arithmetic Operators (cont'd)

HWMod
WS25

numeric_std

Motivation

IEEE Package

Types

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```
1 process is
2   variable u : unsigned(3 downto 0) := "1010";
3   variable s : signed(3 downto 0) := "1010";
4 begin
5   report to_string(resize(u, 5)); -- 01010
6
7
8
9
10
11
12
13
14
15
16   wait;
17 end process;
```

Arithmetic Operators (cont'd)

HWMod
WS25

numeric_std

Motivation

IEEE Package

Types

Operators

Conversion

```
1 process is
2   variable u : unsigned(3 downto 0) := "1010";
3   variable s : signed(3 downto 0) := "1010";
4 begin
5   report to_string(resize(u, 5)); -- 01010
6   report to_string(resize(s, 5)); -- 11010
7
8
9
10
11
12
13
14
15
16   wait;
17 end process;
```

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HWMod
WS25

numeric_std

Motivation

IEEE Package

Types

Operators

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1 process is
2   variable u : unsigned(3 downto 0) := "1010";
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4 begin
5   report to_string(resize(u, 5)); -- 01010
6   report to_string(resize(s, 5)); -- 11010
7
8   report to_string(resize(u, 3));
9
10
11
12
13
14
15
16   wait;
17 end process;
```

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HWMod
WS25

numeric_std

Motivation

IEEE Package

Types

Operators

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7
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9
10
11
12
13
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HWMod
WS25

numeric_std

Motivation

IEEE Package

Types

Operators

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7
8   report to_string(resize(u, 3)); -- 010
9   report to_string(resize(s, 3)); -- 110
10
11
12
13
14
15
16   wait;
17 end process;
```

Arithmetic Operators (cont'd)

HWMod
WS25

numeric_std

Motivation

IEEE Package

Types

Operators

Conversion

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7
8   report to_string(resize(u, 3)); -- 010
9   report to_string(resize(s, 3)); -- 110
10
11   u := u + 1;
12   s := s - 2;
13   if u = 0 or s < -1 then
14     report "HWMod is awesome";
15   end if;
16   wait;
17 end process;
```

Type Conversion

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Conversion function from / to `integer`, type casts between array types

`numeric_std`

Motivation

IEEE Package

Types

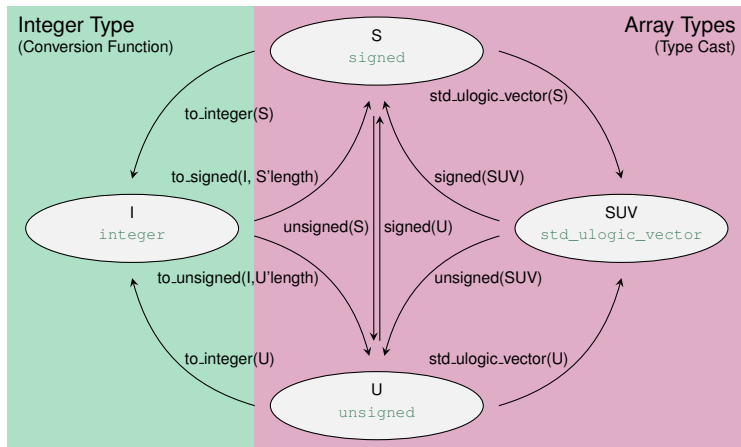
Operators

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Type Conversion

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Lecture Complete!