

Hardware Modeling [VU] (191.011)

– WS25 –

9-Valued Logic and Resolution (IEEE 1164)

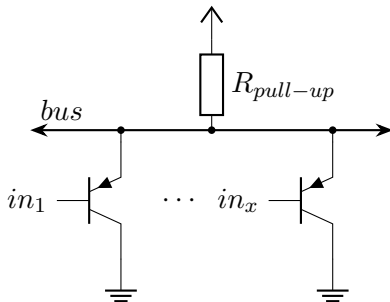
Florian Huemer & Sebastian Wiedemann & Dylan Baumann

WS 2025/26

Motivation | Wired-AND

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■ Example: Wired-AND circuit



IEEE 1164

Motivation

Standard

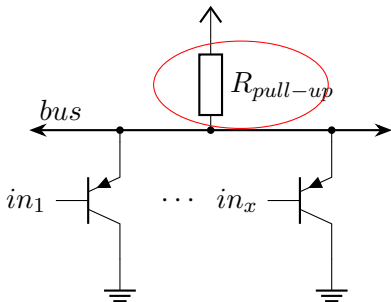
VHDL Types

Resolution

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- Example: Wired-AND circuit
- A pull-up resistor pulls *bus* to HIGH when none of the transistors is active



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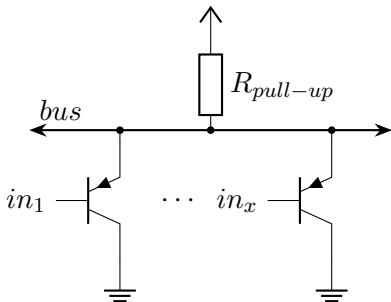
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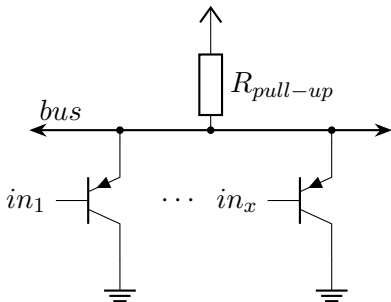
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IEEE 1164
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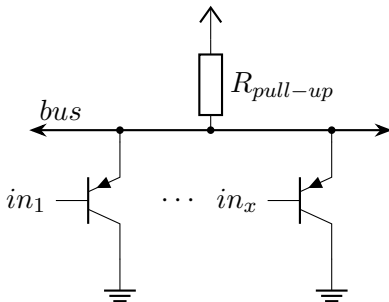


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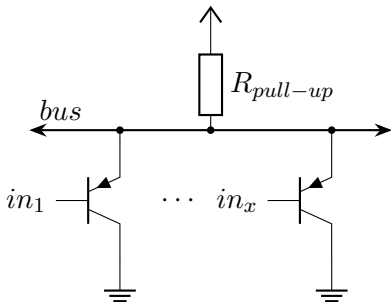


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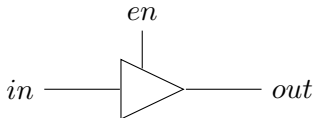


Motivation | Tri-State Buffer

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- Another example: *tri-state* buffer

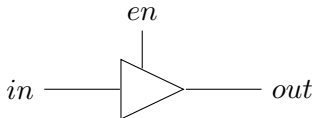


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- Another example: *tri-state* buffer
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Motivation | Tri-State Buffer

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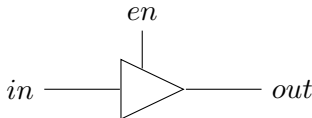
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- $en = 1 \Rightarrow$ buffer is *transparent*: in propagated to out
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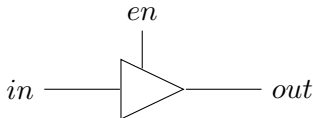


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The IEEE std_logic_1164 package

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IEEE 1164

Motivation

Standard

Package

Value System

VHDL Types

Resolution

- Recall from *Digital Design* lecture: 9-valued logic
 - Contains values for different driver strength / impedance
 - Also values useful for simulation and synthesis

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327

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library ieee;  
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```
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- ⇒ Get access to two 9-valued logic (and related) types:
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IEEE 1164 std_ulogic Type

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■ Simple enumeration type with nine values

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type std_ulogic is ('U', 'X', '0', '1', 'Z', 'W', 'L', 'H', '-');
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VHDL Types

std_ulogic

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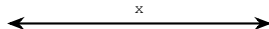
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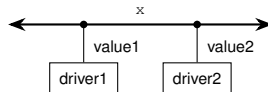
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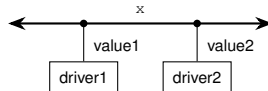
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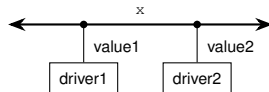
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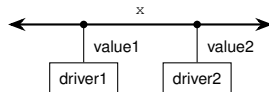
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IEEE 1164 std_logic Type

HWMod
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The std_ulogic Resolution Function

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Resolution

Overview

`std_ulogic`

`RES_TABLE`

- Resolves multiple `std_ulogic` values into a single one

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The std_ulogic Resolution Function

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3 begin
4
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5     return s(s'low);
6   else
7     for i in s'range loop
8       res := RES_TABLE(result, s(i));
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7     for i in s'range loop
8       res := RES_TABLE(result, s(i));
9     end loop;
10  end if;
11  return result;
12 end function;
```

The std_ulogic Resolution Function

HWMod
WS25

IEEE 1164

Motivation

Standard

VHDL Types

Resolution

Overview

std_ulogic

RES_TABLE

- Resolves multiple `std_ulogic` values into a single one 

```
1 function resolved (s : std_ulogic_vector) return std_ulogic is
2   variable result : std_ulogic := 'Z';
3 begin
4   if (s'length = 1) then
5     return s(s'low);
6   else
7     for i in s'range loop
8       res := RES_TABLE(result, s(i));
9     end loop;
10  end if;
11  return result;
12 end function;
```

The std_ulogic Resolution Function (cont'd)

HWMod
WS25

- The RES_TABLE defines how two values are resolved into one

IEEE 1164

Motivation

Standard

VHDL Types

Resolution

Overview

std_ulogic

RES_TABLE

The std_ulogic Resolution Function (cont'd)

HWMod
WS25

- The RES_TABLE defines how two values are resolved into one

```
1 constant RES_TABLE: stdlogic_table := (  
2 -- U    X    0    1    Z    W    L    H    -  
3 -----  
4 ('U','U','U','U','U','U','U','U','U'), -- U  
5 ('U','X','X','X','X','X','X','X','X'), -- X  
6 ('U','X','0','X','0','0','0','0','X'), -- 0  
7 ('U','X','X','1','1','1','1','1','X'), -- 1  
8 ('U','X','0','1','Z','W','L','H','X'), -- Z  
9 ('U','X','0','1','W','W','W','W','X'), -- W  
10 ('U','X','0','1','L','W','L','W','X'), -- L  
11 ('U','X','0','1','H','W','W','H','X'), -- H  
12 ('U','X','X','X','X','X','X','X','X') -- -  
13 );
```

IEEE 1164

Motivation

Standard

VHDL Types

Resolution

Overview

std_ulogic

RES_TABLE

The std_ulogic Resolution Function (cont'd)

HWMod
WS25

- The RES_TABLE defines how two values are resolved into one

```
1 constant RES_TABLE: stdlogic_table := (  
2 -- U    X    0    1    Z    W    L    H    -  
3 -----  
4 ('U','U','U','U','U','U','U','U','U'), -- U  
5 ('U','X','X','X','X','X','X','X','X'), -- X  
6 ('U','X','0','X','0','0','0','0','X'), -- 0  
7 ('U','X','X','1','1','1','1','1','X'), -- 1  
8 ('U','X','0','1','Z','W','L','H','X'), -- Z  
9 ('U','X','0','1','W','W','W','W','X'), -- W  
10 ('U','X','0','1','L','W','L','W','X'), -- L  
11 ('U','X','0','1','H','W','W','H','X'), -- H  
12 ('U','X','X','X','X','X','X','X','X') -- -  
13 );
```

IEEE 1164

Motivation

Standard

VHDL Types

Resolution

Overview

std_ulogic

RES_TABLE

The std_ulogic Resolution Function (cont'd)

HWMod
WS25

- The RES_TABLE defines how two values are resolved into one

```
1 constant RES_TABLE: stdlogic_table := (  
2 -- U    X    0    1    Z    W    L    H    -  
3 -----  
4 ('U','U','U','U','U','U','U','U','U'), -- U  
5 ('U','X','X','X','X','X','X','X','X'), -- X  
6 ('U','X','0','X','0','0','0','0','X'), -- 0  
7 ('U','X','X','1','1','1','1','1','X'), -- 1  
8 ('U','X','0','1','Z','W','L','H','X'), -- Z  
9 ('U','X','0','1','W','W','W','W','X'), -- W  
10 ('U','X','0','1','L','W','L','W','X'), -- L  
11 ('U','X','0','1','H','W','W','H','X'), -- H  
12 ('U','X','X','X','X','X','X','X','X') -- -  
13 );
```

IEEE 1164

Motivation

Standard

VHDL Types

Resolution

Overview

std_ulogic

RES_TABLE

The std_ulogic Resolution Function (cont'd)

HWMod
WS25

- The RES_TABLE defines how two values are resolved into one

```
1 constant RES_TABLE: stdlogic_table := (  
2 -- U    X    0    1    Z    W    L    H    -  
3 -----  
4 ('U','U','U','U','U','U','U','U','U'), -- U  
5 ('U','X','X','X','X','X','X','X','X'), -- X  
6 ('U','X','0','X','0','0','0','0','X'), -- 0  
7 ('U','X','X','1','1','1','1','1','X'), -- 1  
8 ('U','X','0','1','Z','W','L','H','X'), -- Z  
9 ('U','X','0','1','W','W','W','W','X'), -- W  
10 ('U','X','0','1','L','W','L','W','X'), -- L  
11 ('U','X','0','1','H','W','W','H','X'), -- H  
12 ('U','X','X','X','X','X','X','X','X') -- -  
13 );
```

IEEE 1164

Motivation

Standard

VHDL Types

Resolution

Overview

std_ulogic

RES_TABLE

The std_ulogic Resolution Function (cont'd)

HWMod
WS25

- The RES_TABLE defines how two values are resolved into one

```
1 constant RES_TABLE: stdlogic_table := (  
2 -- U    X    0    1    Z    W    L    H    -  
3 -----  
4 ('U','U','U','U','U','U','U','U','U'), -- U  
5 ('U','X','X','X','X','X','X','X','X'), -- X  
6 ('U','X','0','X','0','0','0','0','X'), -- 0  
7 ('U','X','X','1','1','1','1','1','X'), -- 1  
8 ('U','X','0','1','Z','W','L','H','X'), -- Z  
9 ('U','X','0','1','W','W','W','W','X'), -- W  
10 ('U','X','0','1','L','W','L','W','X'), -- L  
11 ('U','X','0','1','H','W','W','H','X'), -- H  
12 ('U','X','X','X','X','X','X','X','X') -- -  
13 );
```

IEEE 1164

Motivation

Standard

VHDL Types

Resolution

Overview

std_ulogic

RES_TABLE

The std_ulogic Resolution Function (cont'd)

HWMod
WS25

IEEE 1164

Motivation

Standard

VHDL Types

Resolution

Overview

std_ulogic

RES_TABLE

- The RES_TABLE defines how two values are resolved into one
Example: pull-up ('H'), active ('0') and inactive ('Z') driver

```
1 constant RES_TABLE: stdlogic_table := (  
2 -- U    X    0    1    Z    W    L    H    -  
3 -----  
4 ('U','U','U','U','U','U','U','U','U'), -- U  
5 ('U','X','X','X','X','X','X','X','X'), -- X  
6 ('U','X','0','X','0','0','0','0','X'), -- 0  
7 ('U','X','X','1','1','1','1','1','X'), -- 1  
8 ('U','X','0','1','Z','W','L','H','X'), -- Z  
9 ('U','X','0','1','W','W','W','W','X'), -- W  
10 ('U','X','0','1','L','W','L','W','X'), -- L  
11 ('U','X','0','1','H','W','W','H','X'), -- H  
12 ('U','X','X','X','X','X','X','X','X') -- -  
13 );
```

resolve("H0Z") :

The std_ulogic Resolution Function (cont'd)

HWMod
WS25

- The RES_TABLE defines how two values are resolved into one
Example: pull-up ('H'), active ('0') and inactive ('Z') driver

```
1 constant RES_TABLE: stdlogic_table := (  
2 -- U    X    0    1    Z    W    L    H    -  
3 -----  
4 ('U','U','U','U','U','U','U','U','U'), -- U  
5 ('U','X','X','X','X','X','X','X','X'), -- X  
6 ('U','X','0','X','0','0','0','0','X'), -- 0  
7 ('U','X','X','1','1','1','1','1','X'), -- 1  
8 ('U','X','0','1','Z','W','L','H','X'), -- Z  
9 ('U','X','0','1','W','W','W','W','X'), -- W  
10 ('U','X','0','1','L','W','L','W','X'), -- L  
11 ('U','X','0','1','H','W','W','H','X'), -- H  
12 ('U','X','X','X','X','X','X','X','X') -- -  
13 );
```

resolve("H0Z") :

1 RES_TABLE('Z', 'H') = 'H'

IEEE 1164

Motivation

Standard

VHDL Types

Resolution

Overview

stdlogic

RES_TABLE

The std_ulogic Resolution Function (cont'd)

HWMod
WS25

IEEE 1164

Motivation

Standard

VHDL Types

Resolution

Overview

std_ulogic

RES_TABLE

- The RES_TABLE defines how two values are resolved into one
Example: pull-up ('H'), active ('0') and inactive ('Z') driver

```
1 constant RES_TABLE: stdlogic_table := (  
2 -- U    X    0    1    Z    W    L    H    -  
3 -----  
4 ('U','U','U','U','U','U','U','U','U'), -- U  
5 ('U','X','X','X','X','X','X','X','X'), -- X  
6 ('U','X','0','X','0','0','0','0','X'), -- 0  
7 ('U','X','X','1','1','1','1','1','X'), -- 1  
8 ('U','X','0','1','Z','W','L','H','X'), -- Z  
9 ('U','X','0','1','W','W','W','W','X'), -- W  
10 ('U','X','0','1','L','W','L','W','X'), -- L  
11 ('U','X','0','1','H','W','W','H','X'), -- H  
12 ('U','X','X','X','X','X','X','X','X') -- -  
13 );
```

resolve("H0Z") :

- 1 RES_TABLE('Z', 'H') = 'H'
- 2 RES_TABLE('H', '0') = '0'

The std_ulogic Resolution Function (cont'd)

HWMod
WS25

- The RES_TABLE defines how two values are resolved into one
Example: pull-up ('H'), active ('0') and inactive ('Z') driver

```
1 constant RES_TABLE: stdlogic_table := (  
2 -- U    X    0    1    Z    W    L    H    -  
3 -----  
4 ('U','U','U','U','U','U','U','U','U'), -- U  
5 ('U','X','X','X','X','X','X','X','X'), -- X  
6 ('U','X','0','X','0','0','0','0','X'), -- 0  
7 ('U','X','X','1','1','1','1','1','X'), -- 1  
8 ('U','X','0','1','Z','W','L','H','X'), -- Z  
9 ('U','X','0','1','W','W','W','W','X'), -- W  
10 ('U','X','0','1','L','W','L','W','X'), -- L  
11 ('U','X','0','1','H','W','W','H','X'), -- H  
12 ('U','X','X','X','X','X','X','X','X') -- -  
13 );
```

resolve("H0Z") :

- 1 RES_TABLE('Z', 'H') = 'H'
- 2 RES_TABLE('H', '0') = '0'
- 3 RES_TABLE('0', 'Z') = '0'

IEEE 1164

Motivation

Standard

VHDL Types

Resolution

Overview

std_ulogic

RES_TABLE

The std_ulogic Resolution Function (cont'd)

HWMod
WS25

IEEE 1164

Motivation

Standard

VHDL Types

Resolution

Overview

std_ulogic

RES_TABLE

- The RES_TABLE defines how two values are resolved into one
Example: pull-up ('H'), active ('0') and inactive ('Z') driver

```
1 constant RES_TABLE: stdlogic_table := (  
2 -- U    X    0    1    Z    W    L    H    -  
3 -----  
4 ('U','U','U','U','U','U','U','U','U'), -- U  
5 ('U','X','X','X','X','X','X','X','X'), -- X  
6 ('U','X','0','X','0','0','0','0','X'), -- 0  
7 ('U','X','X','1','1','1','1','1','X'), -- 1  
8 ('U','X','0','1','Z','W','L','H','X'), -- Z  
9 ('U','X','0','1','W','W','W','W','X'), -- W  
10 ('U','X','0','1','L','W','L','W','X'), -- L  
11 ('U','X','0','1','H','W','W','H','X'), -- H  
12 ('U','X','X','X','X','X','X','X','X') -- -  
13 );
```

resolve("H0Z") :

1 RES_TABLE('Z', 'H') = 'H'

2 RES_TABLE('H', '0') = '0'

3 RES_TABLE('0', 'Z') = '0'

⇒ resolve("H0Z") = '0'

The std_ulogic Resolution Function (cont'd)

HWMod
WS25

IEEE 1164

Motivation

Standard

VHDL Types

Resolution

Overview

std_ulogic

RES_TABLE

- The RES_TABLE defines how two values are resolved into one
Example: pull-up ('H'), active ('0') and inactive ('Z') driver

```
1 constant RES_TABLE: stdlogic_table := (  
2 -- U    X    0    1    Z    W    L    H    -  
3 -----  
4 ('U','U','U','U','U','U','U','U','U'), -- U  
5 ('U','X','X','X','X','X','X','X','X'), -- X  
6 ('U','X','0','X','0','0','0','0','X'), -- 0  
7 ('U','X','X','1','1','1','1','1','X'), -- 1  
8 ('U','X','0','1','Z','W','L','H','X'), -- Z  
9 ('U','X','0','1','W','W','W','W','X'), -- W  
10 ('U','X','0','1','L','W','L','W','X'), -- L  
11 ('U','X','0','1','H','W','W','H','X'), -- H  
12 ('U','X','X','X','X','X','X','X','X') -- -  
13 );
```

resolve("H0Z") :

1 RES_TABLE('Z', 'H') = 'H'

2 RES_TABLE('H', '0') = '0'

3 RES_TABLE('0', 'Z') = '0'

⇒ resolve("H0Z") = '0'

Lecture Complete!