Hardware Modeling [VU] (191.011)
– WS25 –
Metastability

Guest Lecture by Prof. Steininger

WS 2025/26

Modified: 2025-12-16, 16:05 (f8a58e9)

Recap: Synchronous Design

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  - Circuits consist of complex networks of comb. gates
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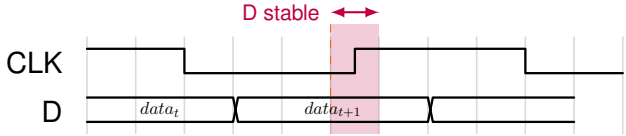
- Flip-flops between combinational logic control signal propagation
- Flip-flops have inherent timing constraints

Flip-Flop Timing Constraints

- Input data must be stable around active clock edge
  - Otherwise not clear which value to capture



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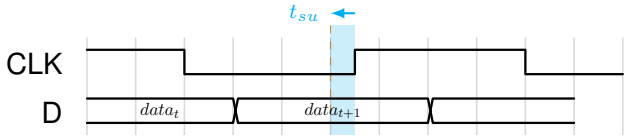

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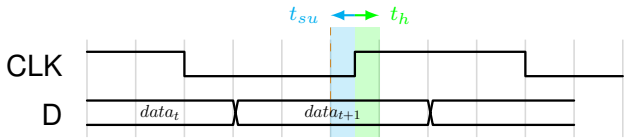

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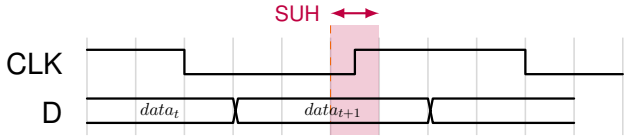
- This is the **setup-hold window** (SUH window)



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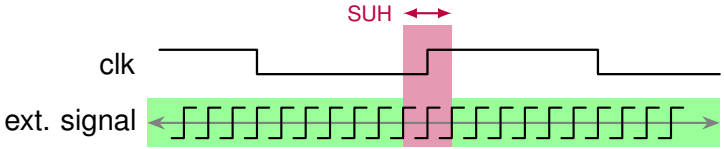
  - In particular: they can arrive within a SUH window



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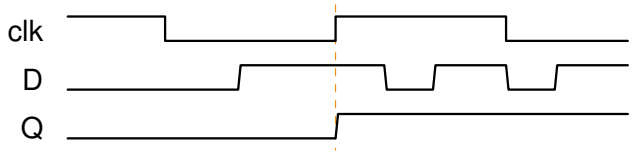
  - Comb. gates: simply produce incomplete results
  - Flip-flop: **Metastability**

Flip-Flop Metastability

- The flip-flop is supposed to assume one of two states after a clock edge
  - State reflected by the output



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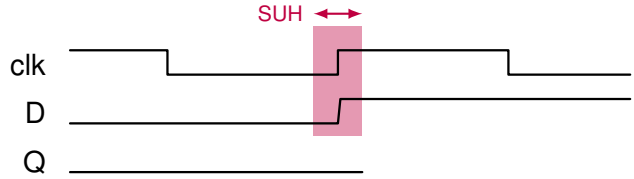

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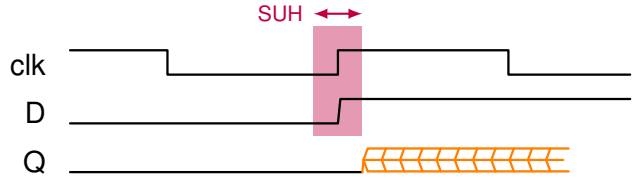

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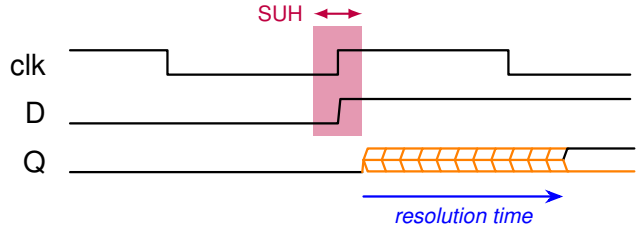
$\Rightarrow$ Flip-flop stay may at intermediate state for some *resolution time*



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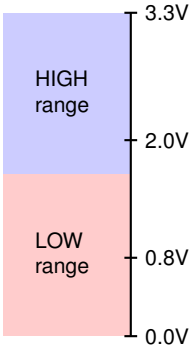
- Inherent to any system with transitions between multiple stable states
- Metastability is the act of *balancing* between stable states
  - Output voltage of FF, elephant on ball...
- In general: Metastability **cannot** be mitigated!
  - Neither resolution time nor final outcome can be determined in advance

Consequences of Metastability in Circuits

- Obtaining binary logic levels by discretizing analog voltage



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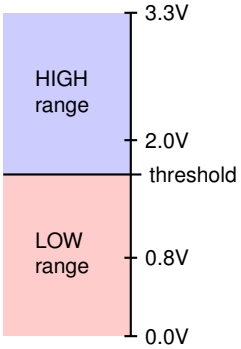

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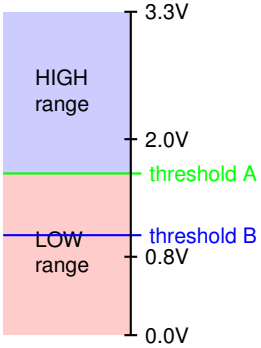

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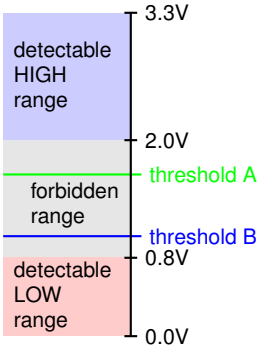

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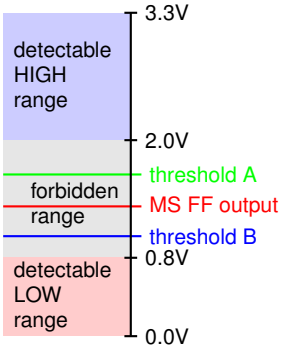

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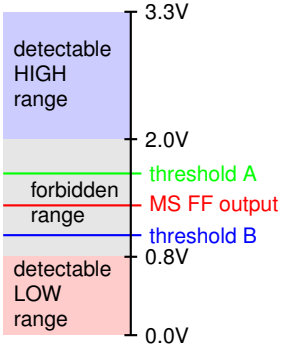

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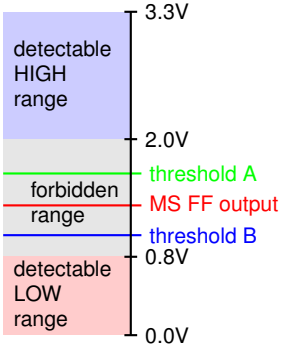
- Late transitions, Glitches, Oscillations



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⇒ *Mean Time Between Upsets* (MTBU)

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