Hardware Modeling [VU] (191.011)
– WS25 –
Metastability

Guest Lecture by Prof. Steininger

WS 2025/26

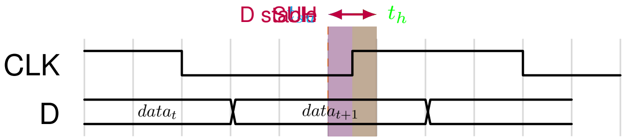
Recap: Synchronous Design

- Hardware usually operates with high concurrency
  - Circuits consist of complex networks of comb. gates
  - Combinational gates immediately react to input changes
- Coordination is required for proper operation
  - Inputs must be stable throughout computation
  - Outputs must be valid when used

$\Rightarrow$ Use a global clock signal as common notion of time
  - Flip-flops between combinational logic control signal propagation
  - Flip-flops have inherent timing constraints

Flip-Flop Timing Constraints

- Input data must be stable around active clock edge
  - Otherwise not clear which value to capture
  - **Setup Time**: specifies how long data must be stable *before* clock edge
  - **Hold Time**: specifies how long data must be stable *after* clock edge
- This is the **setup-hold window** (SUH window)

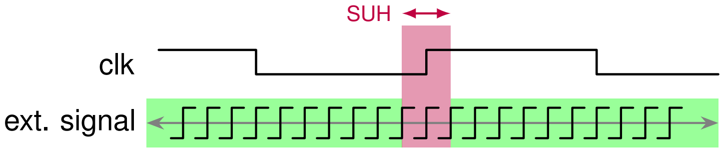


Timing Violations?

- Static timing analysis ensures sufficiently long clock period for all timing constraints of FFs and comb. logic to be satisfied

$\Rightarrow$ Are timing violations then even possible? Why bother?

- Every useful circuit requires an interface to the outside world
  - Transition at external inputs will arrive at *any* time
  - In particular: they can arrive within a SUH window



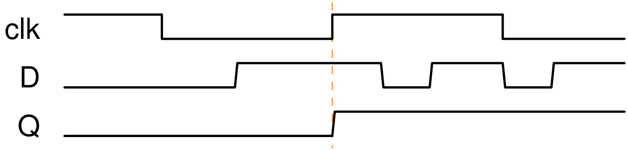
Timing Violations!

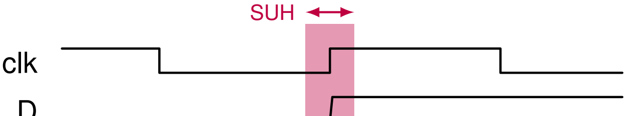
- What happens *if* the timing constraints are violated?
- Distinguish between combinational gates and sequential FFs
  - Comb. gates: simply produce incomplete results
  - Flip-flop: **Metastability**

Flip-Flop Metastability

- The flip-flop is supposed to assume one of two states after a clock edge
  - State reflected by the output
- Transition during SUH window $\Rightarrow$ FF might not able to decide on state
- The FF is *metastable* (i.e., between two stable states)

$\Rightarrow$ Flip-flop stay may at intermediate state for some *resolution time*



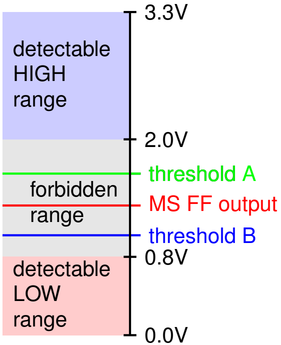


Physical Analogy

- Inherent to any system with transitions between multiple stable states
- Metastability is the act of *balancing* between stable states
  - Output voltage of FF, elephant on ball...
- In general: Metastability **cannot** be mitigated!
  - Neither resolution time nor final outcome can be determined in advance

Consequences of Metastability in Circuits

- Obtaining binary logic levels by discretizing analog voltage
  - Comparison against threshold voltage
- Metastable flip-flop outputs intermediate voltage
- Depending on particular threshold voltages different interpretation
- Late transitions, Glitches, Oscillations



Estimating Effects of Metastability

- MS cannot be mitigated, can we determine how often it causes problems?
- Two contributing factors:
  1. How often input transitions fall within SH window
  2. How often metastability resolves before propagating
- Input transition rate in general uncorrelated to clock $\Rightarrow$ assume uniform distribution of clock-to-data time
- Resolution time not predictable $\Rightarrow$ only statistical estimation possible

$\Rightarrow$ *Mean Time Between Upsets* (MTBU)

$$MTBU = \frac{1}{\lambda_{in} \cdot f_{clk} \cdot T_W} \cdot e^{\frac{t_{res}}{\tau_C}}$$

MTBU Estimation

- MTBU depends on technology and circuit parameters
  - Note: **Rate** of input transitions
  - Exponential influence of t_{res} on MTBU!
- Where does this formula come from? Consider upset rate (UR)
  1. How often input transitions fall within SH window
  2. How often metastability resolves before propagating
- Formula applicable for *uncorrelated* input data **only**!

$$MTBU = \frac{1}{\lambda_{in} \cdot f_{clk} \cdot T_W} \cdot e^{\frac{t_{res}}{\tau_C}}$$

$$\frac{1}{MTBU} = UR = \lambda_{in} \cdot \frac{T_W}{T_{clk}} \cdot e^{-\frac{t_{res}}{\tau_C}}$$

input transition rate (λ_{in})

clock frequency (f_{clk})

FF parameter (T_W, τ_C)

time to resolve (t_{res})

proportion of MS cases not resolving in time ($e^{-\frac{t_{res}}{\tau_C}}$)

avg. rate of transitions within SH window ($\lambda_{in} \cdot \frac{T_W}{T_{clk}}$)

Lecture Complete!