Hardware Modeling [VU] (191.011)
– WS25 –

Sequential Circuit Example: LFSR

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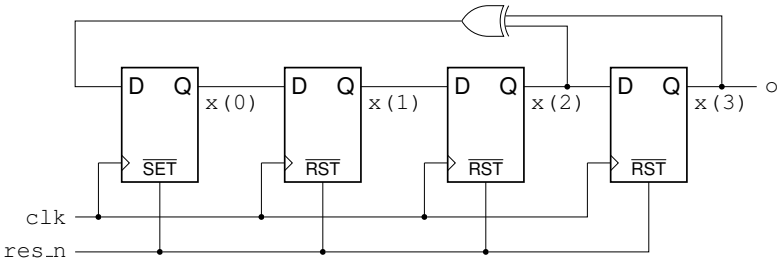
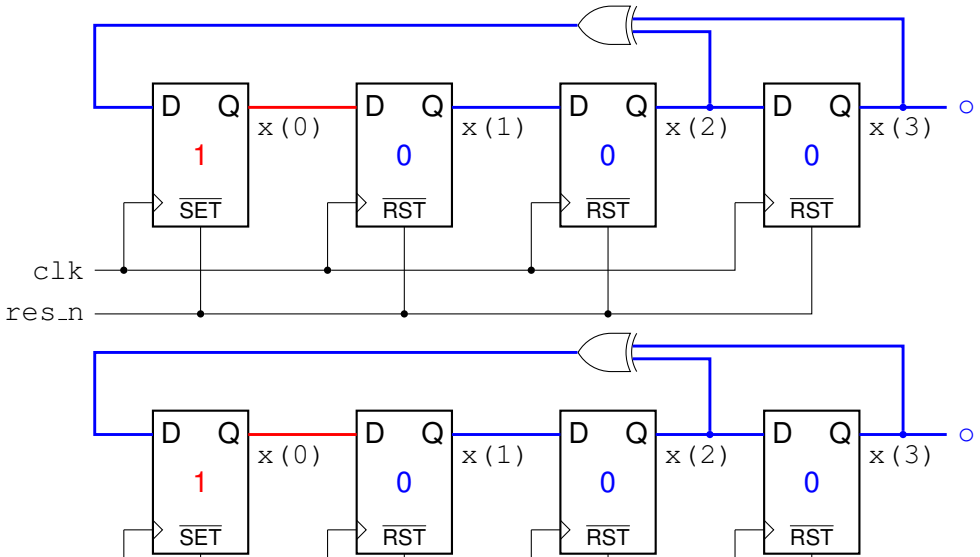
Example: 4-bit LFSR

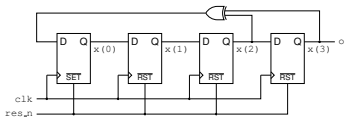


- **L**inear **F**eedback **S**hift **R**egister
- Chain of FFs (*shift-register*) fed by linear combination of its current state
- Pseudo-random sequence of bits

LFSR - Circuit Operation Principle



LFSR - VHDL Design




```vhdl
entity lfsr is
  port (
    clk   : in  std_ulogic;
    res_n : in  std_ulogic;
    o     : out std_ulogic
  );
end entity;
```

```vhdl
architecture arch of lfsr is
  signal x : std_ulogic_vector(0 to 3);
begin









end architecture;
```

LFSR - Testbench


```
1  architecture bench of lfsr_tb is
2    signal clk : std_ulogic;
3    signal res_n : std_ulogic;
4    signal o :  std_ulogic;
5
6
7
8  begin
9
10   uut : entity work.lfsr
11   port map (
12     clk => clk,
13     res_n => res_n,
14     o => o
15   );
```

```
1   clkgen : process
2   begin
3     while not stop_clk loop
4       clk <= '0';
5       wait for 0.5*CLK_PERIOD;
6       clk <= '1';
7       wait for 0.5*CLK_PERIOD;
8     end loop;
9     wait;
10  end process;
```

Lecture Complete!