Hardware Modeling [VU] (191.011)
– WS25 –

Latches and combinational loops

Florian Huemer & Sebastian Wiedemann & Dylan Baumann

WS 2025/26

Modified: 2025-12-16, 16:03 (f8a58e9)

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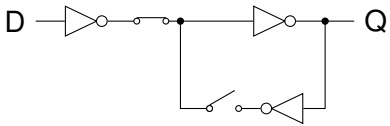

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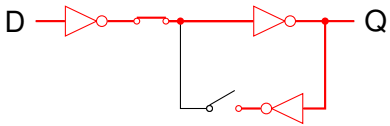

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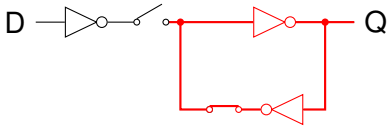

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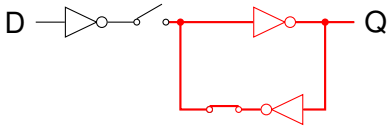

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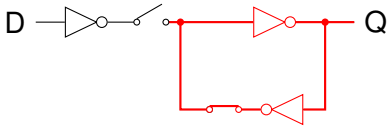

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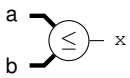


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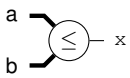


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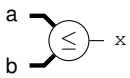


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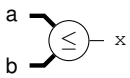


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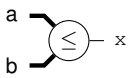
  - Default assignment or `others`
- Detected during synthesis
  - **Never** ignore warnings!

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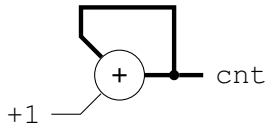

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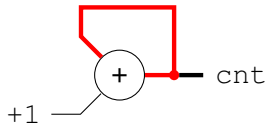

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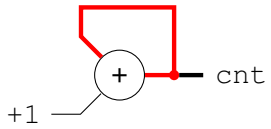

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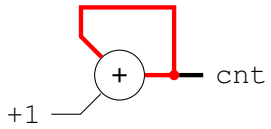

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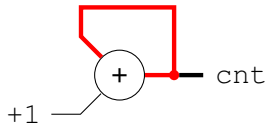

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- Comb. process must never read **and** write to same signal
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- Also reported during synthesis

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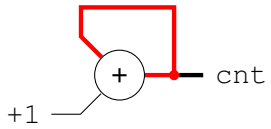

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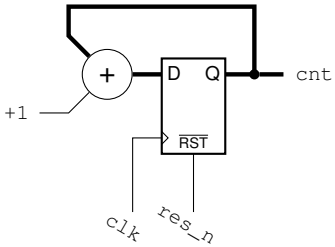

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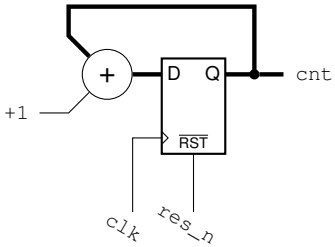

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- Never ignore tool warnings!

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10631 VHDL Process Statement warning at top_arch.vhd(13): inferring latch(es) for signal or variable "abc", which holds its previous value in one or more paths through the process

332125 Found combinational loop of 2 nodes
```

Lecture Complete!