Hardware Modeling [VU] (191.011)
– WS25 –
Latches and combinational loops

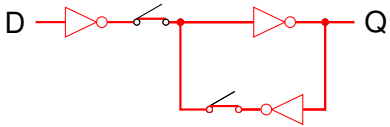
Florian Huemer & Sebastian Wiedemann & Dylan Baumann

WS 2025/26

Modified: 2025-12-16, 16:07 (f8a58e9)

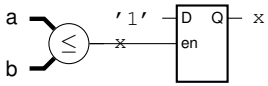
Undesired Latches

- When should you use a latch or a flip-flop?
- In this course latches are **always** undesired
- Often not available as primitive building blocks
  - Built from combinational elements instead
  - Delay of feedback path can become high
  - Feedback path can lead to oscillation



Pitfalls - Latch Errors (cont'd)

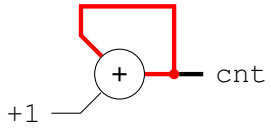
- How do latches *happen*?
  - Not all paths write to signal
  - Holding state ⇒ infer latch
- Always cover all paths/cases!
  - Default assignment or `others`
- Detected during synthesis
  - **Never** ignore warnings!




```
1  entity cmp is
2    port(
3      a, b : in  unsigned;
4      x    : out std_ulogic
5    );
6  end entity;
7
8  architecture arch of cmp is
9  begin
10   main : process (all) begin
11
12     if a <= b then
13       x <= '1';
14     end if;
15   end process;
16 end architecture;
```

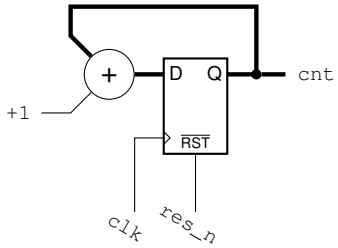
Pitfalls - Combinational Loops

- Feedback loops not exclusive to latches
- Comb. process must never read **and** write to same signal
  - Hard to spot at interfaces
  - Feedback paths must contain flip-flops
- Also reported during synthesis



Pitfalls - Combinational Loops (cnt'd)


```
1  architecture sync of counter is
2    signal cnt, cnt_next : unsigned(7 downto 0);
3  begin
4
5
6
7
8
9
10
11
12
13
14
15 end architecture;
```



Summary

- Latches
  - Often due to missing default values
- Comb. loops
  - Never read **and** write same signal
- Never ignore tool warnings!

```
10631 VHDL Process Statement warning at top_arch.vhd(13): inferring latch(es) for signal or variable "abc", which holds its previous value in one or more paths through the process

332125 Found combinational loop of 2 nodes
```

Lecture Complete!