

Hardware Modeling [VU] (191.011)

– WS25 –

Vectors and Bit String Literals (IEEE 1164)

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Recall: 9-valued Logic and Resolution Functions

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Vector Types
Conclusion

- Boolean logic cannot express different driver strengths

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 - *Unresolved*: `std_ulogic` IEEE SA
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 - *Resolved*: `std_logic` IEEE SA
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- And when do you use which?

Logical Operators

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Example: `and` operator

```
1 constant and_table : stdlogic_table := (
2   U   X   0   1   Z   W   L   H   -
3   -----
4   ('U','U','0','U','U','0','U','U'), -- U
5   ('U','X','0','X','X','0','X','X'), -- X
6   ('0','0','0','0','0','0','0','0'), -- 0
7   ('U','X','0','1','X','X','0','1','X'), -- 1
8   ('U','X','0','X','X','0','X','X'), -- Z
9   ('U','X','0','X','X','0','X','X'), -- W
10  ('0','0','0','0','0','0','0','0'), -- L
11  ('U','X','0','1','X','X','0','1','X'), -- H
12  ('U','X','0','X','X','0','X','X')  -- -
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- The standard also defines arrays of the new types, called vectors

std_[u]logic_vector Types

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type std_ulegic_vector is array (natural range <>) of std_ulegic; IEEE SA  
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std_[u]logic_vector Logical Operators

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 - From and to `bit_vector`
 - To differently encoded strings:
`to_bstring`, `to_ostring`, `to_hstring`

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std_ulogic vs. std_logic

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std_ulogic vs. std_logic

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- When should which type be used?
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- When should which type be used?
- Use unresolved types whenever modelled circuit has a single driver
 - Allow tools to detect undesired multiple drivers
- Most tool generated code and resources use the resolved types

std_ulogic vs. std_logic

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Operators
Vector Types
Conclusion

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 - Allow tools to detect undesired multiple drivers
- Most tool generated code and resources use the resolved types

std_ulogic vs. std_logic

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 - `std_logic_vector` subtype of `std_ulogic_vector` since VHDL 2008

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Lecture Complete!