Hardware Modeling [VU] (191.011)
– WS25 –

Introduction to Hardware Design

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WS 2025/26

Modified: 2025-12-16, 16:03 (f8a58e9)

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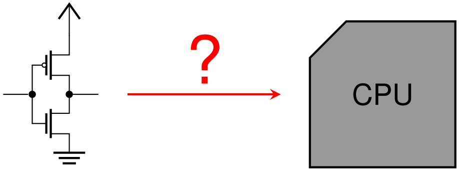

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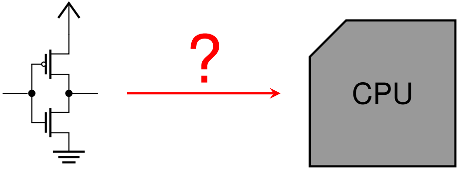

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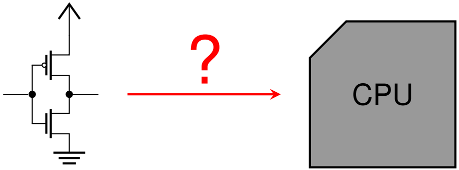
⇒ Hardware Modeling



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  - Up to **billions** of transistors
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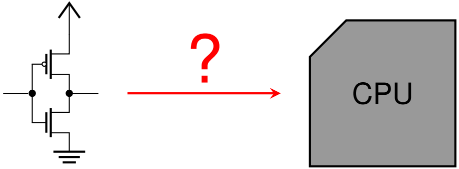
⇒ Hardware Modeling
  - Tools and techniques to bridge the gap



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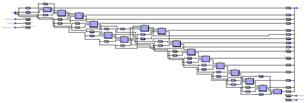

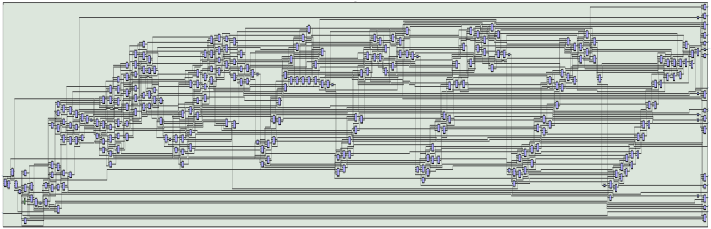

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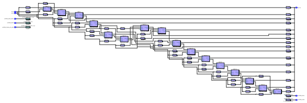

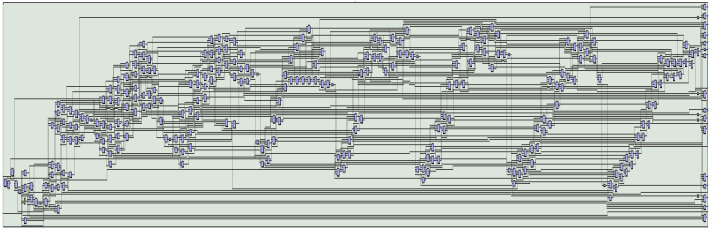

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- Become a better programmer
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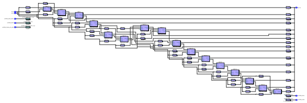
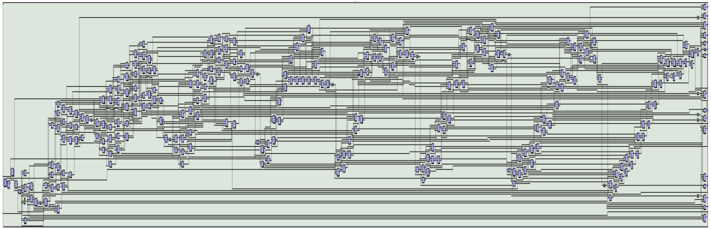
  - Know which knobs to turn
  - New way of thinking
- Example: addition and division in same technology





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Takeaway

This duality makes hardware design hard but also rewarding

Comparison to Software Design (Cont’d)

- Software

- Hardware

Comparison to Software Design (Cont’d)

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```
if (x > y)
  z = x * y;
else
  z = x + y;
return z;
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Comparison to Software Design (Cont'd)

- Software
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  - Either multiplication or addition

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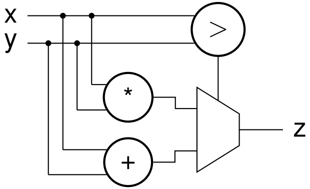

Comparison to Software Design (Cont’d)

- Software
  - Sequential execution
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- Hardware
  - Computations done concurrently
  - All operations always active

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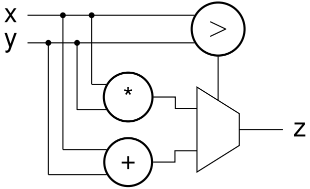

Gajski Y-Chart

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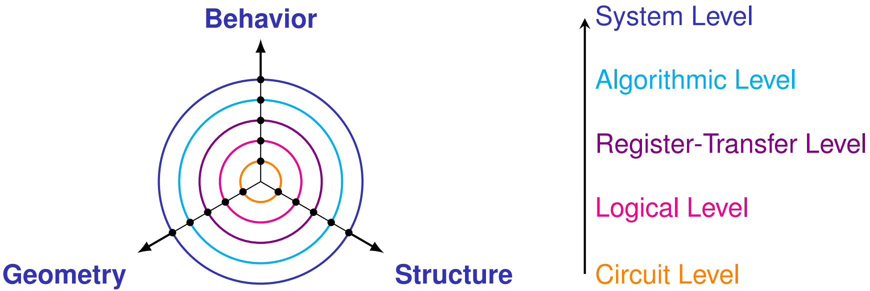

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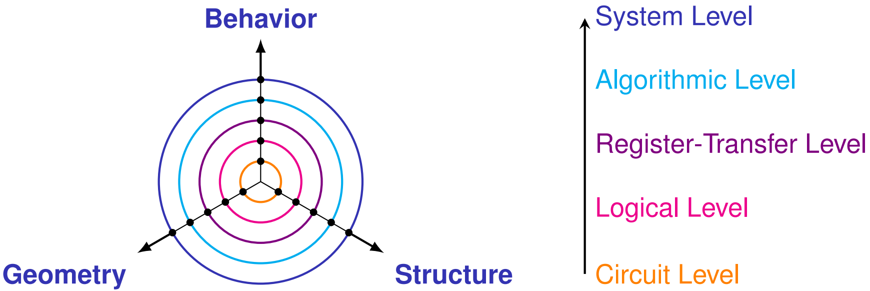

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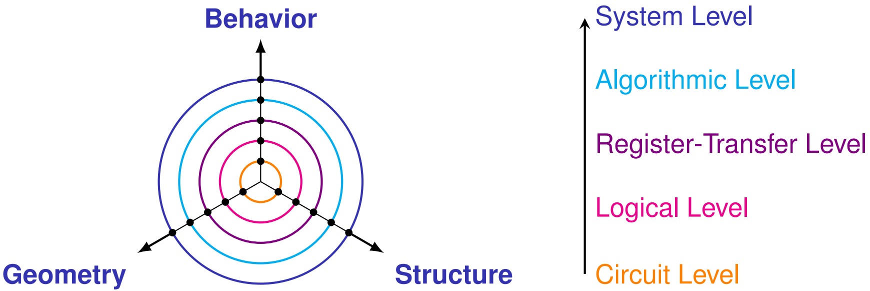

Behavior

Geometry

Structure

System Level

Algorithmic Level

Register-Transfer Level

Logical Level

Circuit Level

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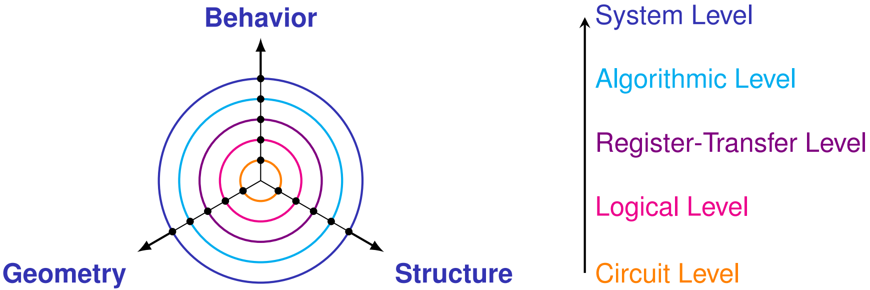

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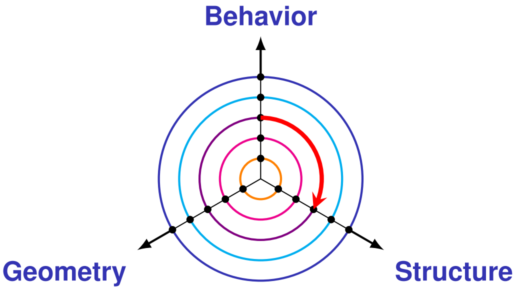

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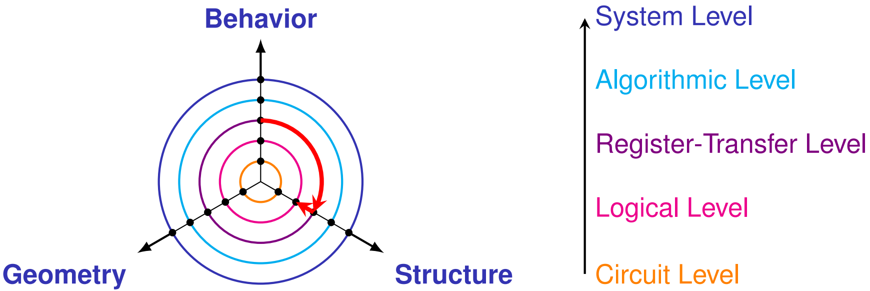

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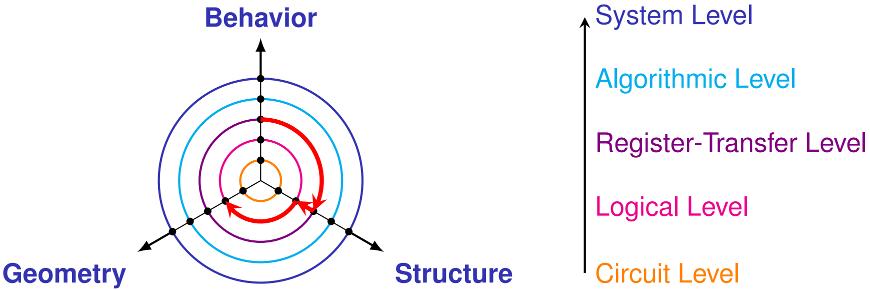

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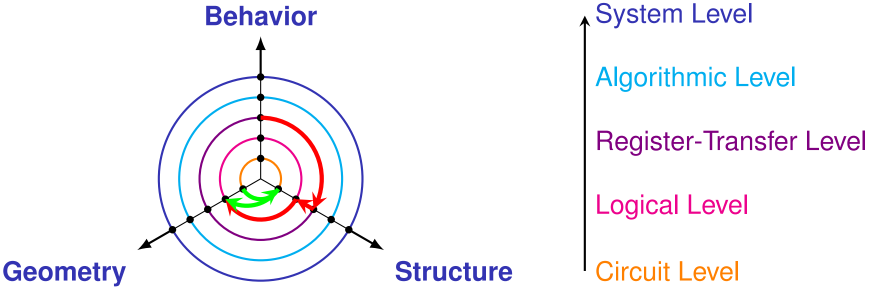

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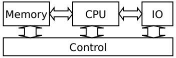
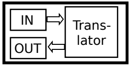
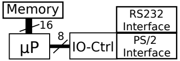
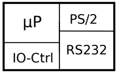
System Level	Inputs : Keyboard Output: Display Function:		
Algorithmic Level	while input read English text translate to German output German Text	 Memory 16 8 µP IO-Ctrl RS232 Interface PS/2 Interface	

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		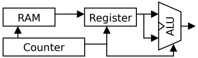	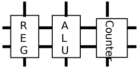

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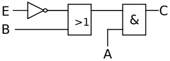
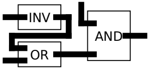
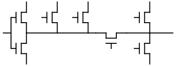
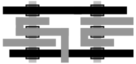
			

Circuit Level	$\frac{dU}{dt} = R\frac{dI}{dt} + \frac{I}{C} + L\frac{d^2I}{dt^2}$		

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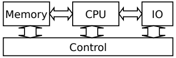
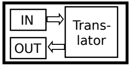
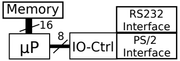
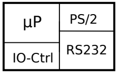
System Level	Inputs : Keyboard Output: Display Function:		
Algorithmic Level	while input read English text translate to German output German Text		

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		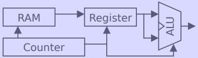	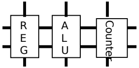

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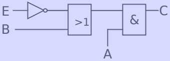
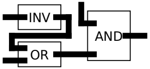
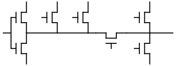
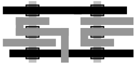
			

Circuit Level	$\frac{dU}{dt} = R\frac{dI}{dt} + \frac{I}{C} + L\frac{d^2I}{dt^2}$		

HDLs

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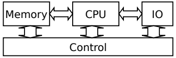
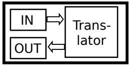
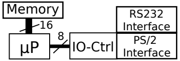
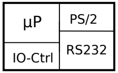
System Level	Inputs : Keyboard Output: Display Function:		
Algorithmic Level	while input read English text translate to German output German Text		

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		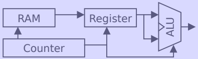	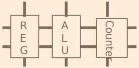

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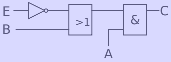
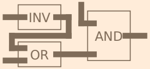
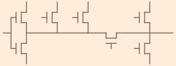
			

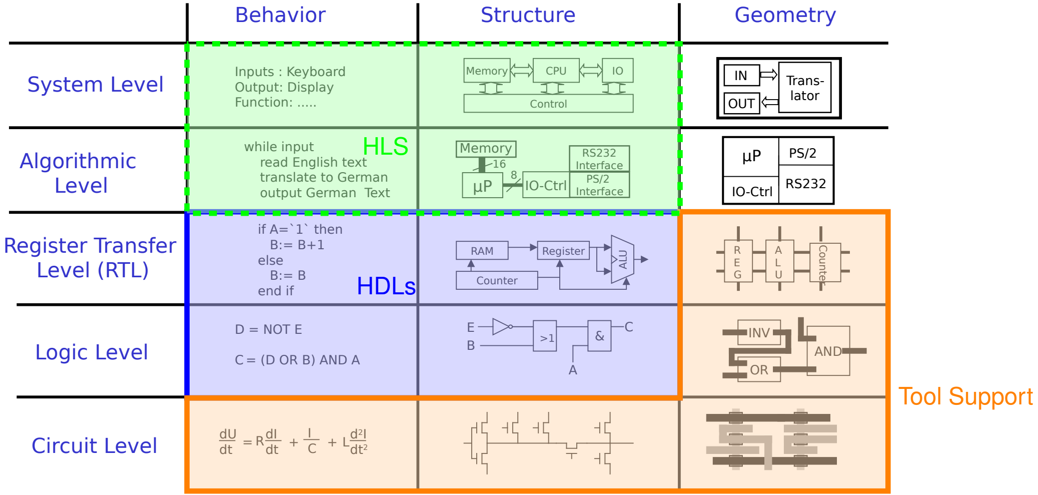
Circuit Level	$\frac{dU}{dt} = R\frac{dI}{dt} + \frac{I}{C} + L\frac{d^2I}{dt^2}$		

Memory
CPU
IO
Control
IN
OUT
Trans-lator
Memory
16
8
µP
IO-Ctrl
RS232 Interface
PS/2 Interface
µP
PS/2
IO-Ctrl
RS232
RAM
Register
ALU
Counter
REG
ALU
Counter
E
B
>1
&
C
A
INV
AND
OR

HDLs

Tool Support

Y-Table



	Behavior	Structure	Geometry
System Level	Inputs : Keyboard Output: Display Function:	Memory CPU IO Control	IN OUT Trans-lator
Algorithmic Level	while input read English text translate to German output German Text	Memory 16 8 µP IO-Ctrl RS232 Interface PS/2 Interface	µP PS/2 IO-Ctrl RS232

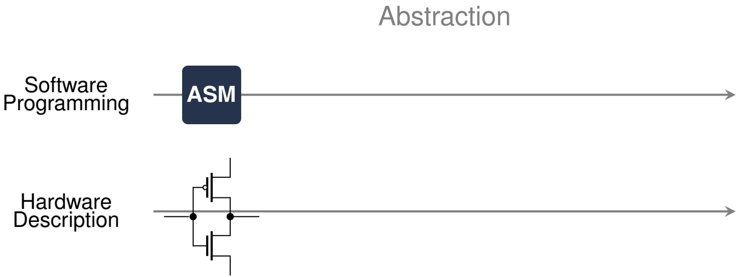
Register Transfer Level (RTL)	if A=`1` then
	B:= B+1
	else
	B:= B
	end if
		RAM
		Register
		Counter
		ALU
			REG
			ALU
			Counter

Logic Level	D = NOT E
	C = (D OR B) AND A
		E
		B
		>1
		&
		C
		A
			INV
			AND
			OR

Circuit Level	$\frac{dU}{dt} = R\frac{dI}{dt} + \frac{I}{C} + L\frac{d^2I}{dt^2}$		

Hardware Description Languages

- Drawing circuits does not scale



Abstraction

Software Programming

ASM

Hardware Description

Hardware Description Languages

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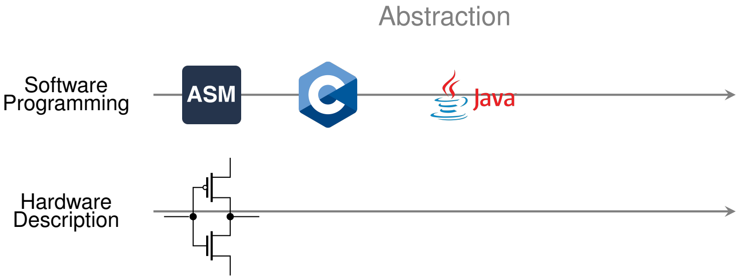
  - Require more abstract method



Hardware Description Languages

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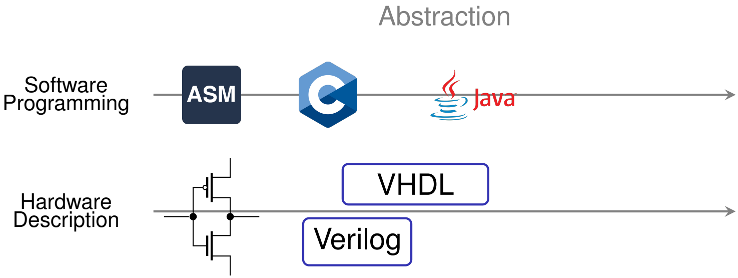
⇒ *Hardware Description Languages* (HDLs)
  - Most popular: VHDL, (System)Verilog



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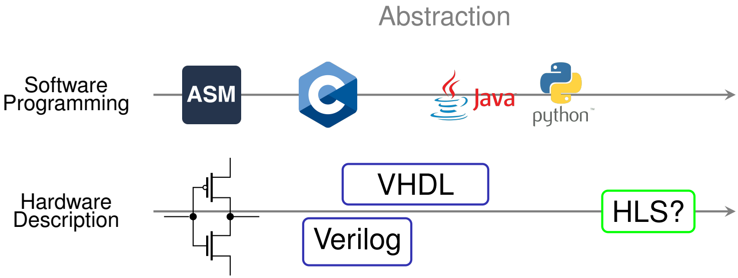

Abstraction

Software Programming

Hardware Description

VHDL

Verilog

HLS?

Hardware Description Languages

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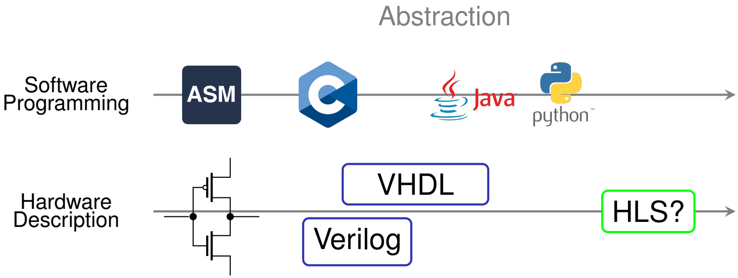

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- The latest VHDL standard (2019) can be found here

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