

Hardware Modeling [VU] (191.011)

– WS25 –

Finite-State Machine Modeling

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WS 2025/26

Motivation

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FSM Modeling

Motivation

Models

Examples

- Why not simply draw circuits?

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FSM Modeling

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- Why not simply draw circuits?
 - Error-prone and scaling poorly for complex FSMs

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FSM Modeling

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- Why not simply draw circuits?
 - Error-prone and scaling poorly for complex FSMs
 - Hard to understand and maintain

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FSM Modeling

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- Why not simply draw circuits?
 - Error-prone and scaling poorly for complex FSMs
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⇒ Increase level of abstraction of description

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- Why not simply draw circuits?

- Error-prone and scaling poorly for complex FSMs
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⇒ Increase level of abstraction of description

- Draw FSMs as graphs (nodes for states, edges for transitions)

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FSM Modeling

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- Why not simply draw circuits?
 - Error-prone and scaling poorly for complex FSMs
 - Hard to understand and maintain
- ⇒ Increase level of abstraction of description
 - Draw FSMs as graphs (nodes for states, edges for transitions)
 - Implementation derived by tools

Common FSM Model

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Behavior Description

The `simple_timer` module keeps an internal `N`-bit counter that is (synchronously) incremented as long as `en` is asserted. When the counter reaches its maximum value ($2^N - 1$) it overflows back to zero. If the counter hits its maximum and `en` is asserted the `tick` output is asserted.

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• counter := 0...00
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• counter := 0...00
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  tick := 0
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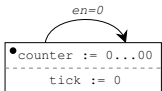
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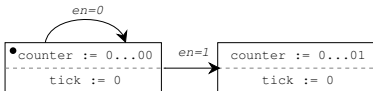
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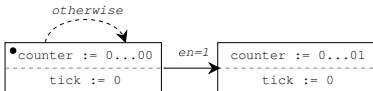
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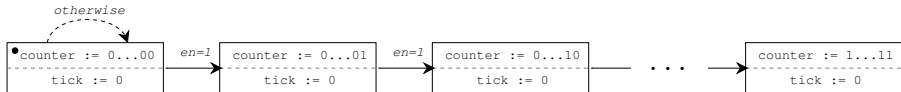
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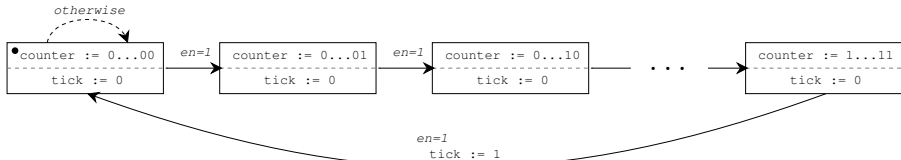
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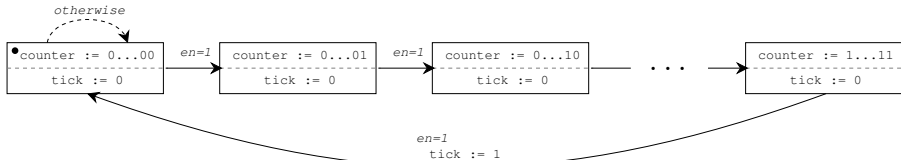
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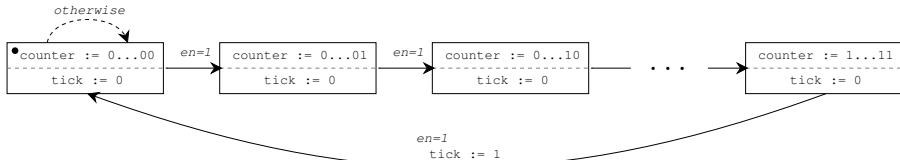
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2^N states $\Rightarrow$ Scaling poorly! (“state explosion”)

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■ Need more abstract FSM model

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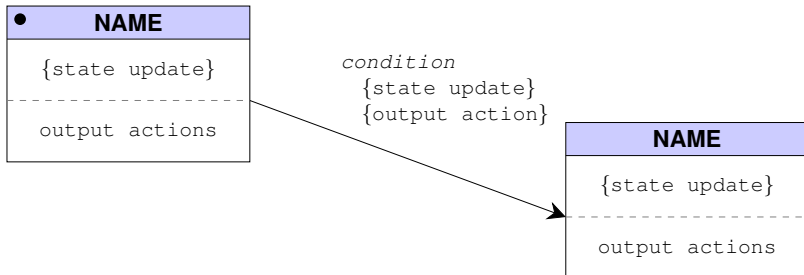
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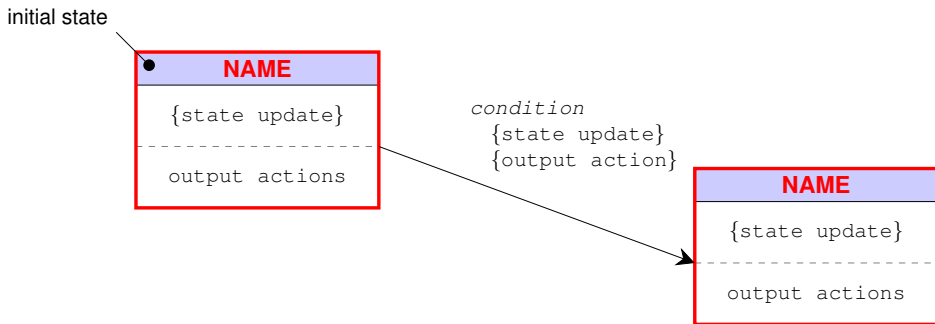
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Examples

- Need more abstract FSM model
 - “Abstract states” gather multiple states with similar behavior



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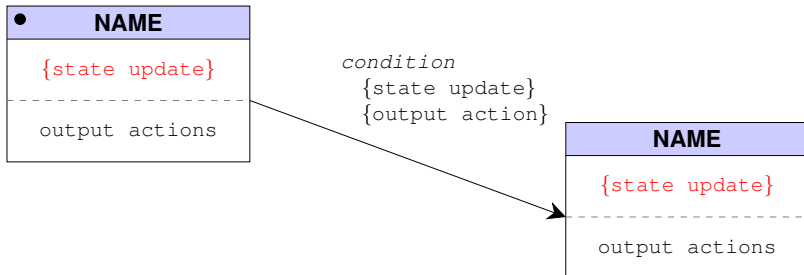
Models

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Examples

- Need more abstract FSM model
 - Optional assignment to state register; per default value unchanged



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- Need more abstract FSM model
 - Mapping of each state to an output

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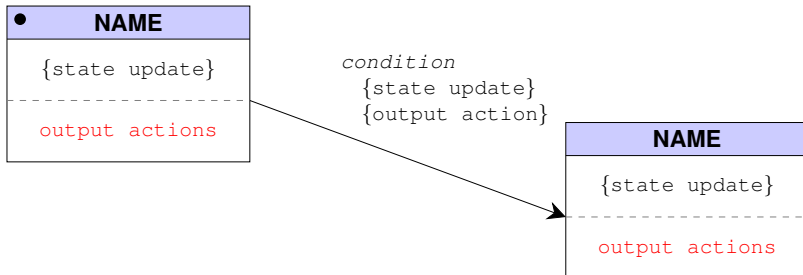
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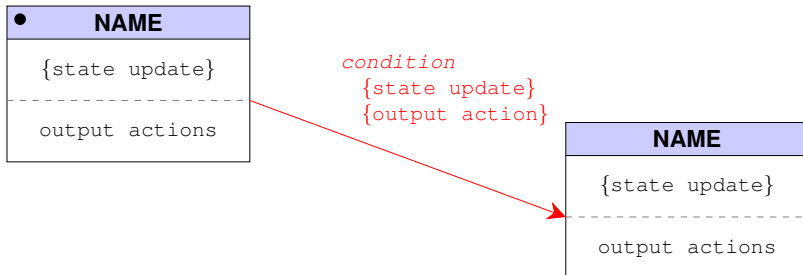
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Examples

- Need more abstract FSM model
 - Conditional state transitions; implicit *otherwise* self-loop if not exhaustive
 - Optional assignments to state register and outputs; overriding node's actions



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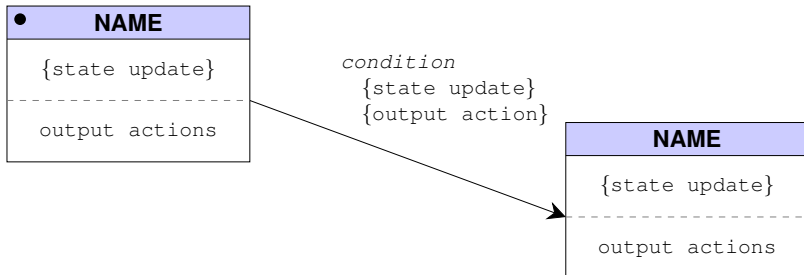
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Examples

- Need more abstract FSM model
 - Conditional state transitions; implicit *otherwise* self-loop if not exhaustive
 - Optional assignments to state register and outputs; overriding node's actions
- Mealy when transition output action depends on input



Example I: `simple_timer`

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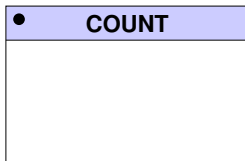
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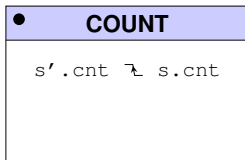
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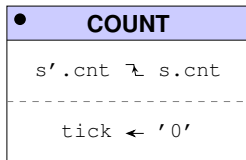
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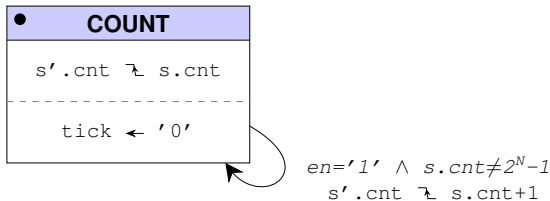
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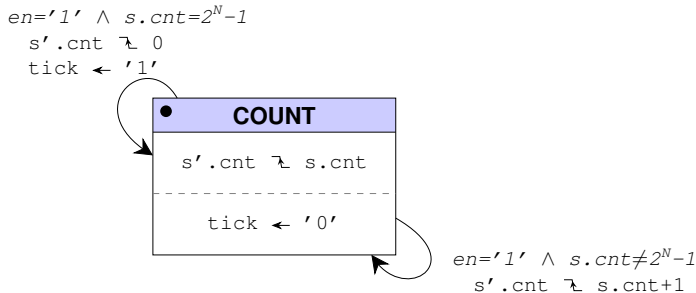
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Synchronous FSM Behavior

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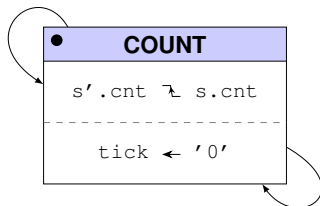
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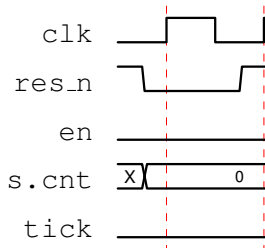
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advanced_timer

$en = '1' \wedge s.cnt = 2^N - 1$
 $s'.cnt \leftarrow 0$
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$en = '1' \wedge s.cnt \neq 2^N - 1$
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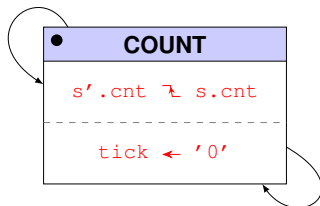
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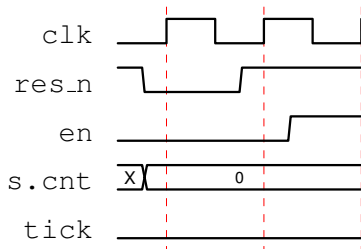
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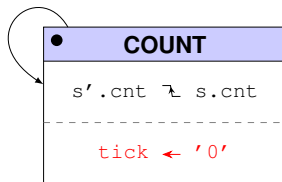
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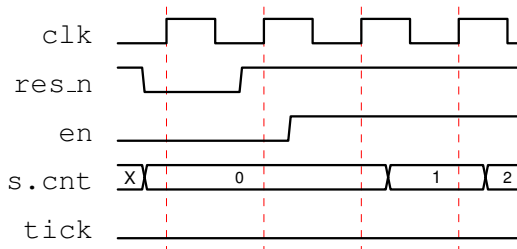
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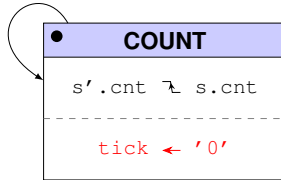
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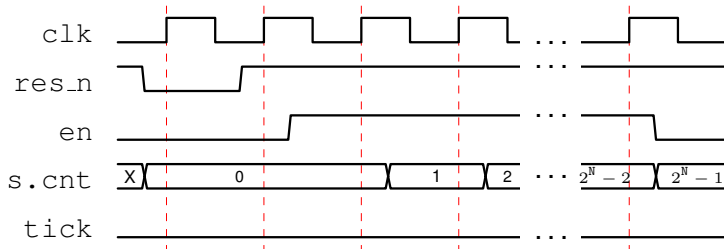
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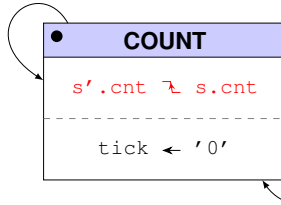
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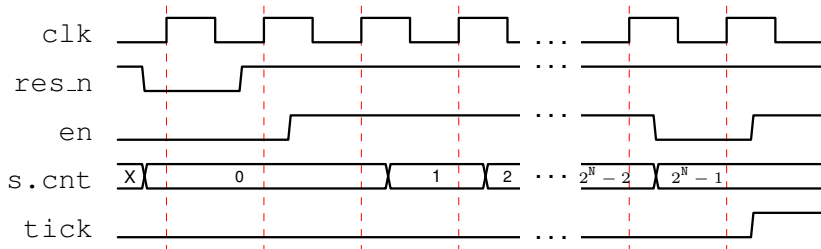
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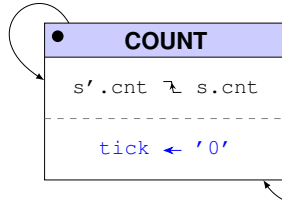
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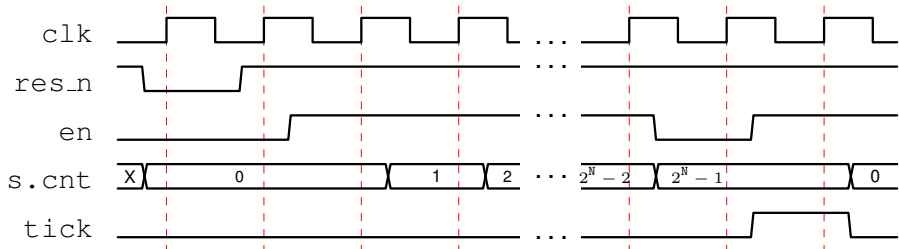
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Example II: `advanced_timer`

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Behavior Description

After a press of button `btn_n` the synchronous `advanced_timer` module starts counting from zero to 15 seconds (inclusive). It shall display the current second as hex value on the seven-segment display `hex`. Before the button press and after it finished counting, the seven-segment display shall be turned off.

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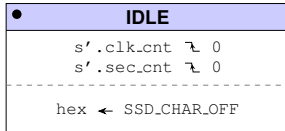
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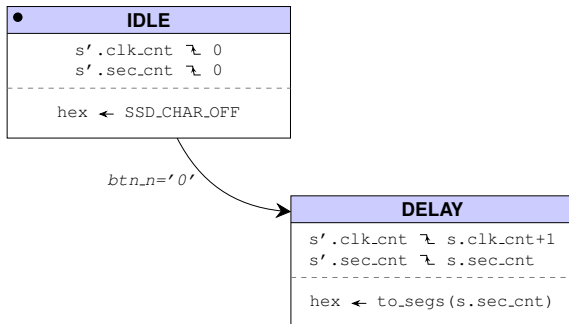
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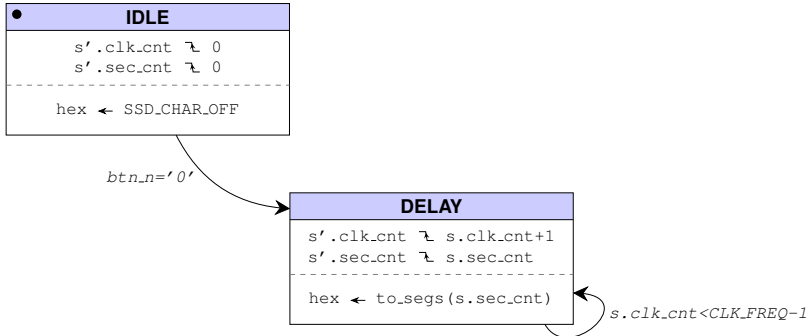
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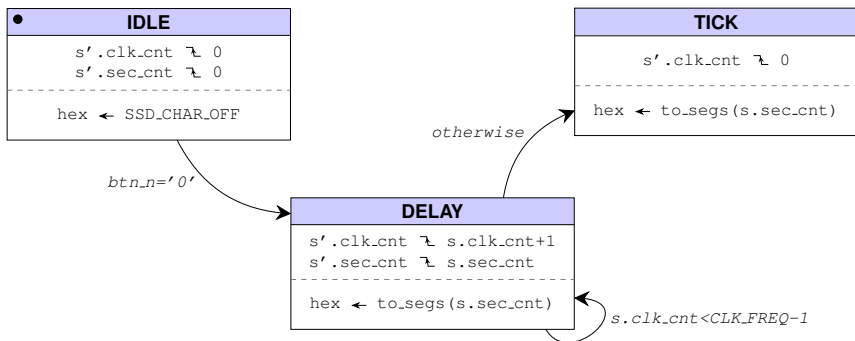
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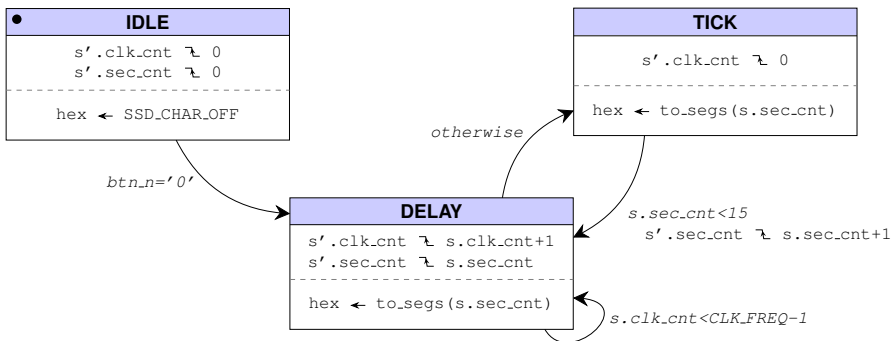
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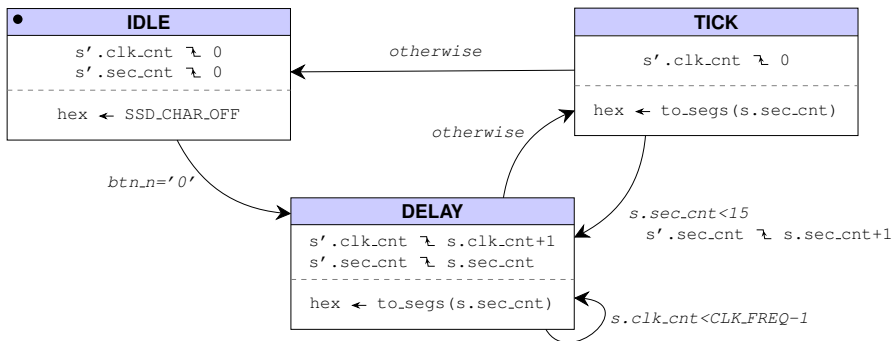
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Lecture Complete!