Hardware Modeling [VU] (191.011)
– WS25 –
Finite-State Machine Modeling

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Motivation

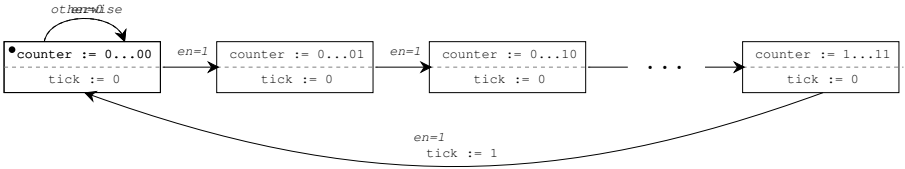
- Why not simply draw circuits?
  - Error-prone and scaling poorly for complex FSMs
  - Hard to understand and maintain

$\Rightarrow$ Increase level of abstraction of description
  - Draw FSMs as graphs (nodes for states, edges for transitions)
  - Implementation derived by tools

Common FSM Model

Behavior Description

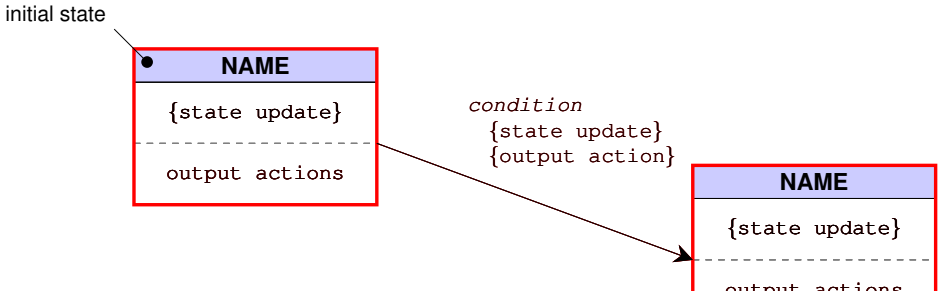
The `simple_timer` module keeps an internal `N`-bit counter that is (synchronously) incremented as long as `en` is asserted. When the counter reaches its maximum value ($2^N - 1$) it overflows back to zero. If the counter hits its maximum and `en` is asserted the `tick` output is asserted.



2^N states$\Rightarrow$ Scaling poorly! (“state explosion”)

HWMod FSM Model

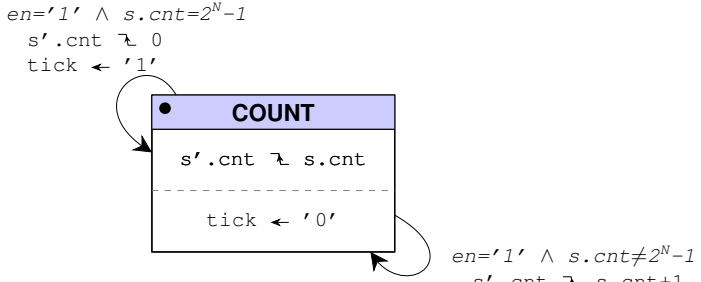
- Need more abstract FSM model
  - “Abstract states” gather multiple states with similar behavior Optional assignment to state register; per default value unchanged Mapping of each state to an output Conditional state transitions; implicit `otherwise` self-loop if not exhaustive
  - Optional assignments to state register and outputs; overriding node’s actions
- Mealy when transition output action depends on input



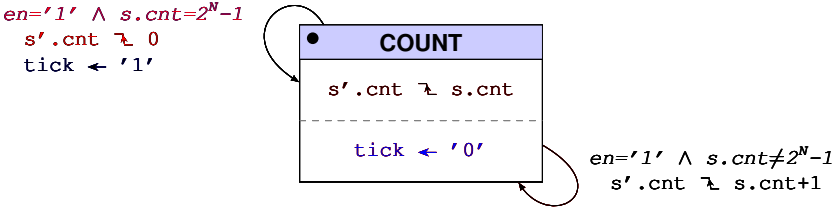
Example I: simple_timer

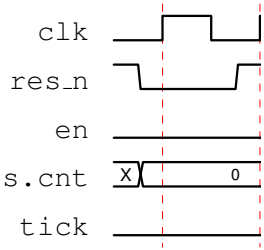
Behavior Description

The simple_timer module keeps an internal N-bit counter that is (synchronously) incremented as long as en is asserted. When the counter reaches its maximum value ($2^N - 1$) it overflows back to zero. If counter hits its maximum and en is asserted the tick output is asserted.



Synchronous FSM Behavior

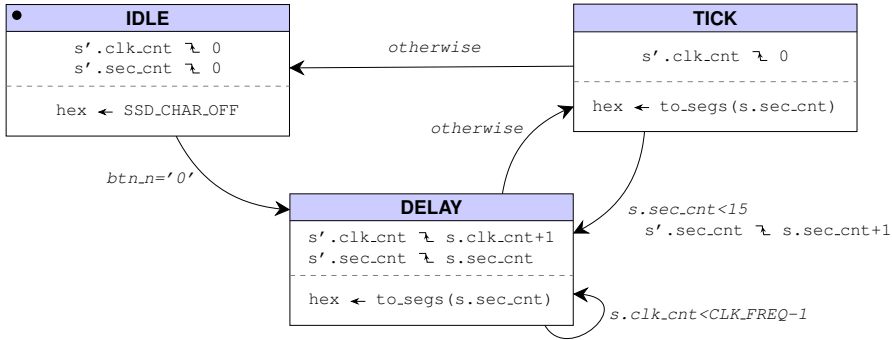




Example II: advanced_timer

Behavior Description

After a press of button btn_n the synchronous advanced_timer module starts counting from zero to 15 seconds (inclusive). It shall display the current second as hex value on the seven-segment display hex. Before the button press and after it finished counting, the seven-segment display shall be turned off.



Lecture Complete!