Hardware Modeling [VU] (191.011)
– WS25 –
VHDL Delay Mechanisms

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WS 2025/26

Modified: 2025-12-16, 16:04 (f8a58e9)

Introduction

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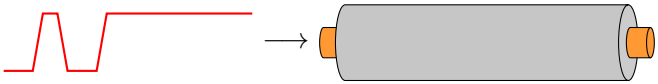
  - Why is this needed? $\Rightarrow$ Delays exist in real hardware
- Two types of delay
  - *Pure* delay: finite signal propagation speed
  - *Inertial* delay: (dis)charging of capacitance

Pure Delay

Pure Delay



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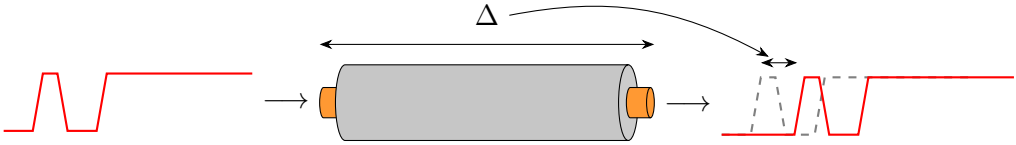

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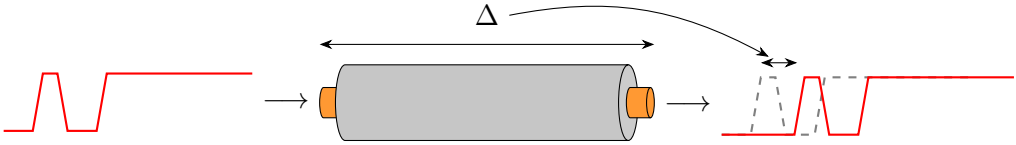

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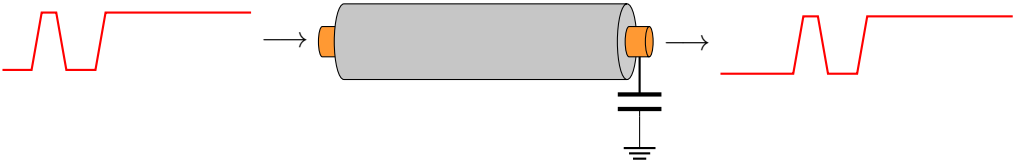

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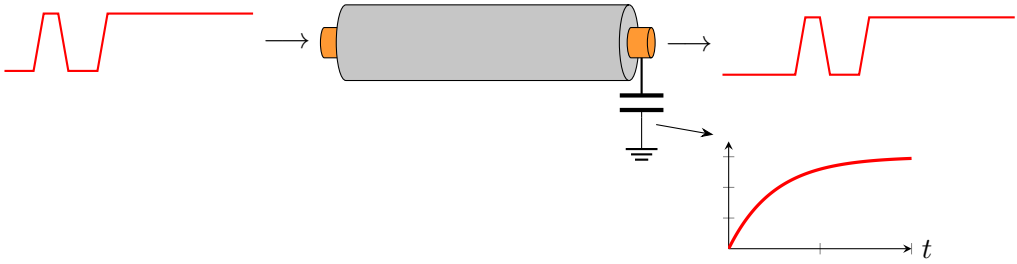

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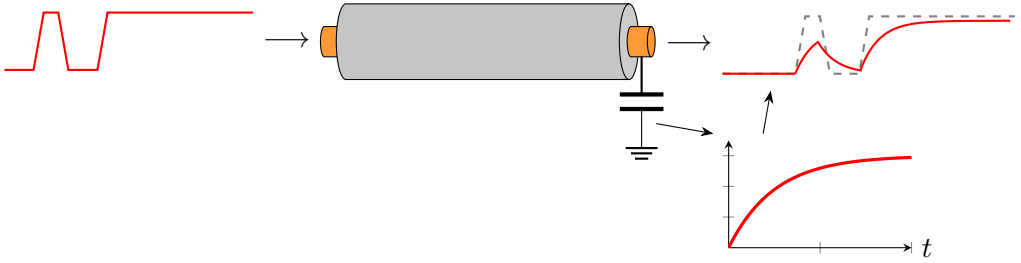

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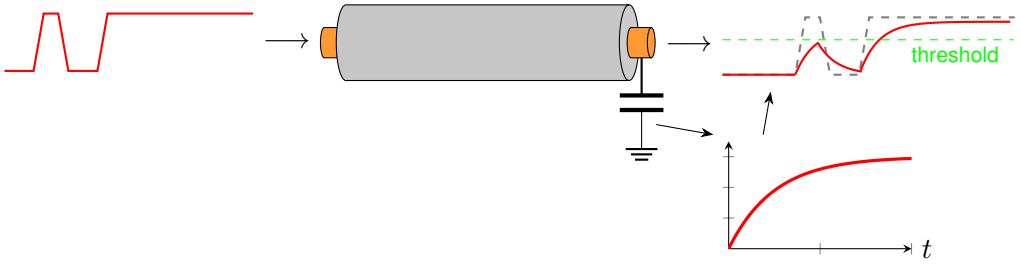

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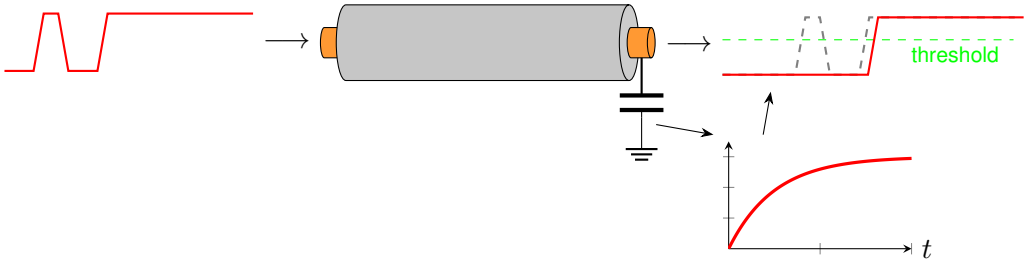

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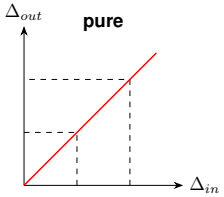

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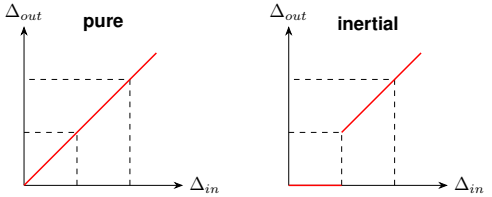

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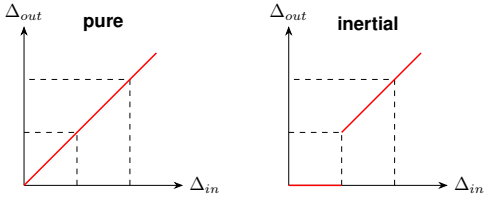
- Further, more specialized, models exist



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  - Supports inertial delay via `reject` and `inertial`

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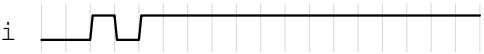

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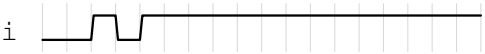

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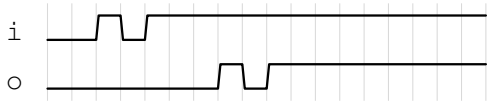

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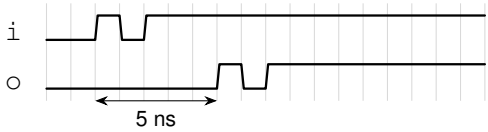

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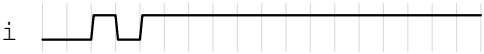

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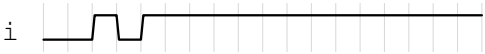

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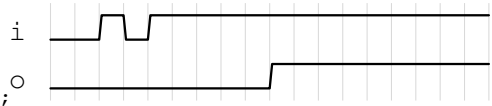

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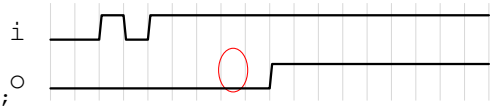

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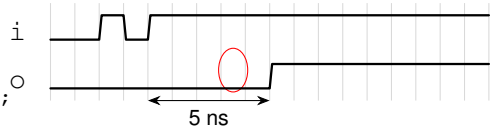

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- Pure delay: can convert to equivalent `inertial` delay

```
o <= transport i after 10 ns;
o <= reject 0 ns inertial i after 10 ns;
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Lecture Complete!