Hardware Modeling [VU] (191.011)
– WS25 –

From Circuits to Code and Back

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WS 2025/26

Modified: 2025-12-16, 16:04 (f8a58e9)

Introduction

Lecture Goal

Develop an intuition for how VHDL code maps to hardware and the associated circuit complexity.

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- Two examples
  - Circuit diagram → Derive VHDL code
  - VHDL code → Derive circuit diagram

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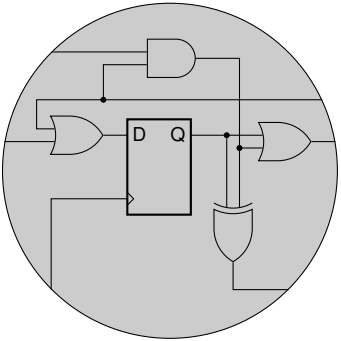
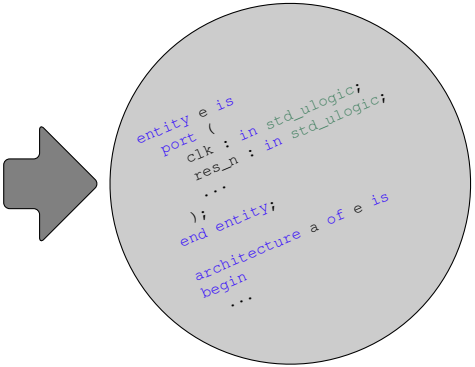
Develop an intuition for how VHDL code maps to hardware and the associated circuit complexity.

- Two examples
  - Circuit diagram → Derive VHDL code
  - VHDL code → Derive circuit diagram
- Important VHDL concepts used in the lecture
  - Sequential circuit elements
  - Behavioral modeling
  - Array-types and arithmetic functions

Example 1: Circuit → VHDL Code

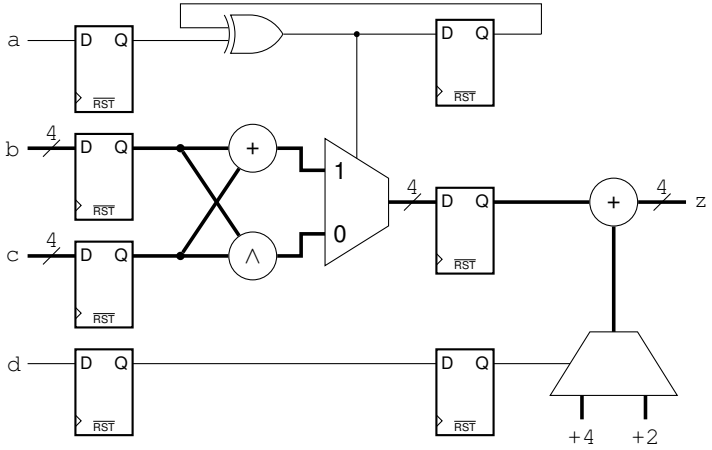




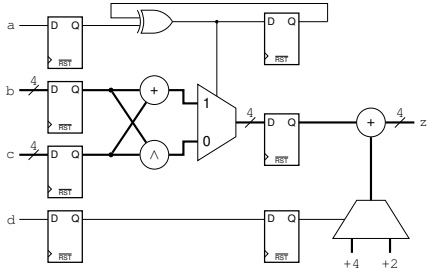
```
entity e is
  port (
    clk : in std_ulogic;
    res_n : in std_ulogic;
    ...
  );
end entity;

architecture a of e is
begin
  ...
```

Example 1: Circuit Diagram



Example 1 - Entity

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1  entity circuit2code is
2    port (
3      clk : in std_ulogic;
4      res_n : in std_ulogic;
5      a : in std_ulogic;
6      b : in std_ulogic_vector(3 downto 0);
7      c : in std_ulogic_vector(3 downto 0);
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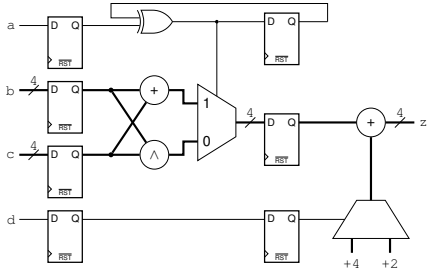


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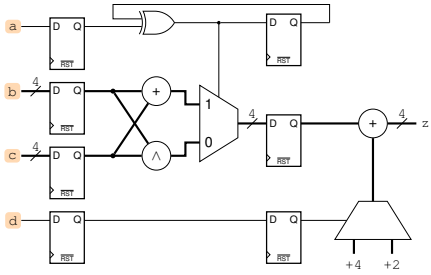


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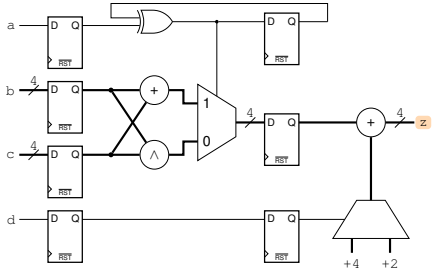


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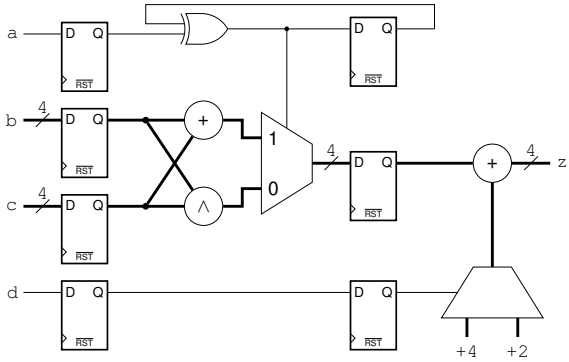

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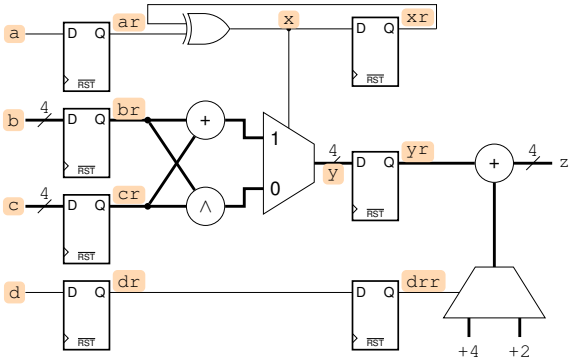

Circuit Preparation

Label **all** register inputs and outputs and other important signals!

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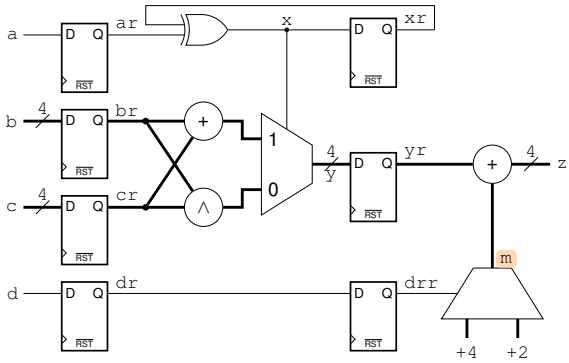

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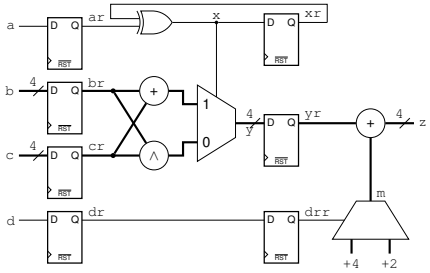
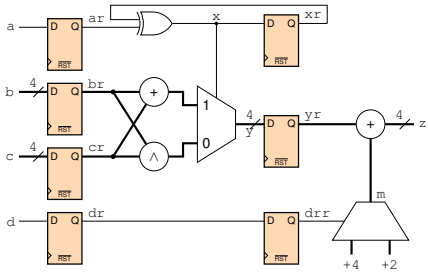
Architecture - Signal Declarations




```
1 architecture arch of circuit2code is
2   signal br, cr, y, yr :
3     std_ulogic_vector(3 downto 0);
4   signal ar, x, xr, dr, drr : std_ulogic;
5 begin
```

Architecture - Registers




```
6   process (clk, res_n)
7   begin
8     if res_n = '0' then
9       ar <= '0'; dr <= '0';
10      xr <= '0'; drr <= '0';
11      br <= (others => '0');
12      cr <= (others => '0');
13      yr <= (others => '0');
14    elsif rising_edge(clk) then
15      ar <= a;
16      br <= b;
17      cr <= c;
18      dr <= d;
19      xr <= x;
20      yr <= y;
21      drr <= dr;
22    end if;
23  end process;
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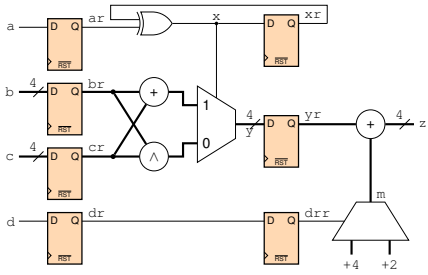


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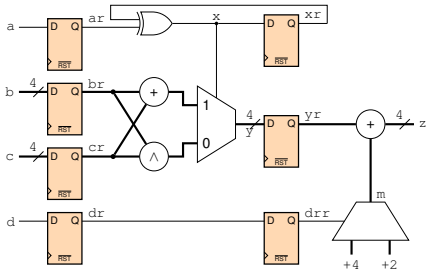


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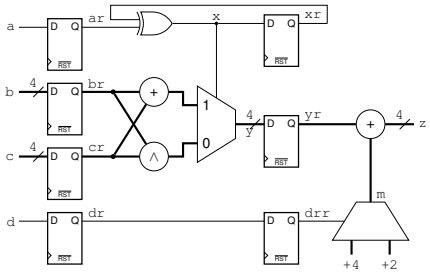
Architecture - Combinational Logic I

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24  x <= ar xor xr;
25
26  process (all)
27  begin
28    if x = '1' then
29      y <= std_ulogic_vector(
30        unsigned(br) +
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33    else
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35    end if;
36  end process;
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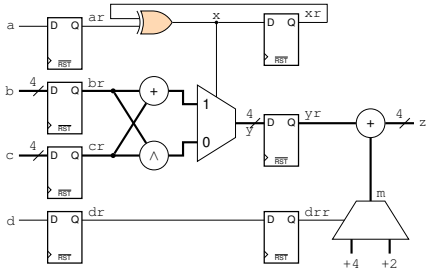


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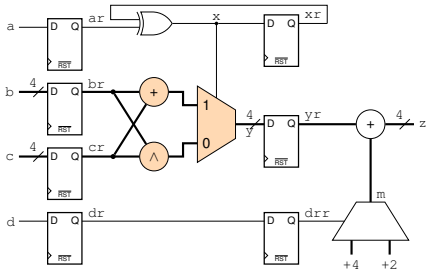


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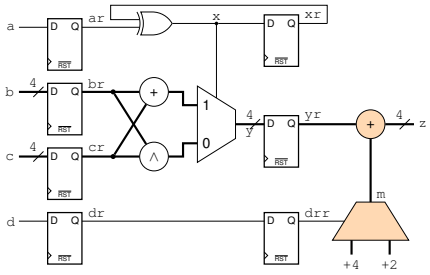


```
37   process (all)
38     variable m : integer;
39   begin
40     if drr = '1' then
41       m := 2;
42     else
43       m := 4;
44     end if;
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46     z <= std_ulogic_vector(
47       unsigned(yr) + m
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49   end process;
50 end architecture;
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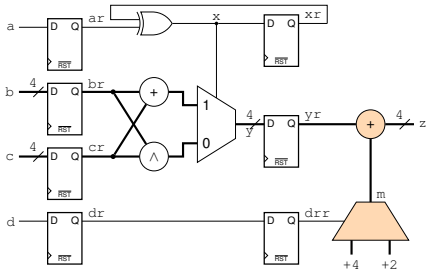


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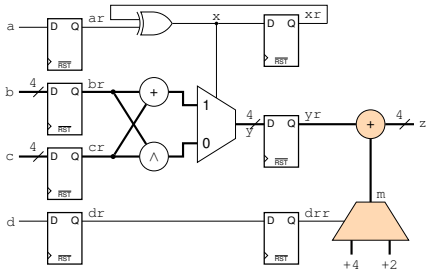


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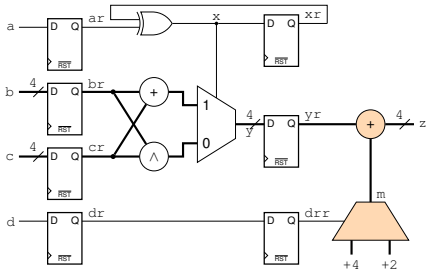


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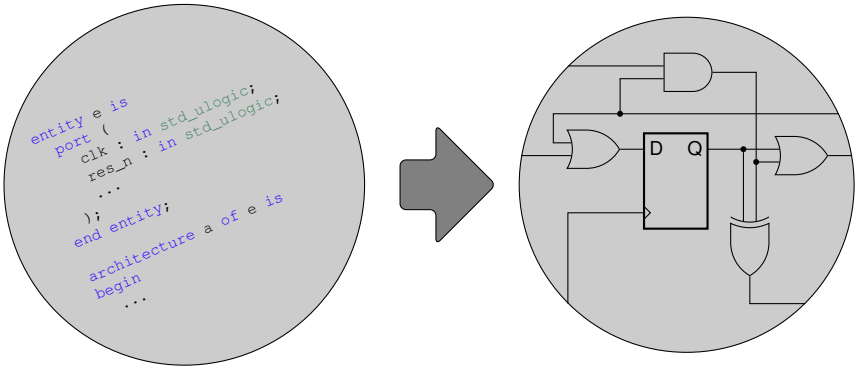
Example 2: VHDL Code → Circuit



Example 2: Entity


```
1  entity code2circuit is
2    generic (
3      N, M : positive
4    );
5    port (
6      clk : in std_ulogic;
7      res_n : in std_ulogic;
8      a : in std_ulogic;
9      b : in std_ulogic_vector(N-1 downto 0);
10     c : in std_ulogic_vector(M-1 downto 0);
11     d : in std_ulogic_vector(M-1 downto 0);
12     x : out std_ulogic;
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14   );
15 end entity;
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10     c : in std_ulogic_vector(M-1 downto 0);
11     d : in std_ulogic_vector(M-1 downto 0);
12     x : out std_ulogic;
13     y : out std_ulogic_vector(M-1 downto 0)
14   );
15 end entity;
```

Example 2: Entity


```
1  entity code2circuit is
2    generic (
3      N, M : positive
4    );
5    port (
6      clk : in std_ulogic;
7      res_n : in std_ulogic;
8      a : in std_ulogic;
9      b : in std_ulogic_vector(N-1 downto 0);
10     c : in std_ulogic_vector(M-1 downto 0);
11     d : in std_ulogic_vector(M-1 downto 0);
12     x : out std_ulogic;
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Example 2: Entity


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Example 2: Architecture


```
1  architecture arch of code2circuit is
2    signal r0, r1 : std_ulogic;
3    signal r2 : c'subtype;
4  begin
5    process (clk, res_n)
6    begin
7      if res_n = '0' then
8        r0 <= '0'; r1 <= '0'; x <= '0';
9        r2 <= (others => '0');
10     elsif rising_edge(clk) then
11       r0 <= a xor r1;
12       r1 <= r0;
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17     end if;
18   end process;
19   process(all)
20     variable temp : std_ulogic;
21   begin
22     temp := '0';
23     for i in b'range loop
24       temp := temp or b(i);
25     end loop;
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27     y <= r2;
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29     if temp and r0 then
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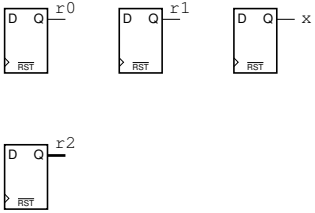

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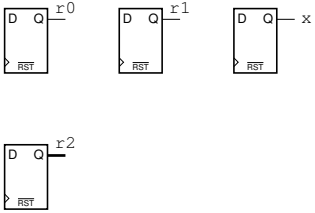

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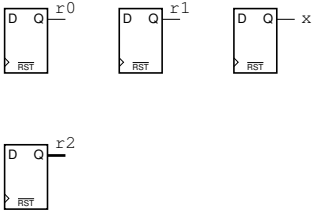

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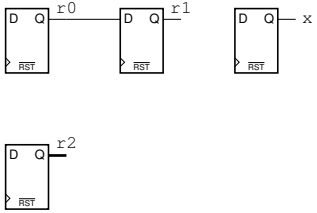

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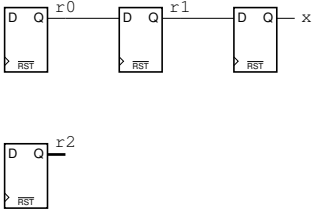

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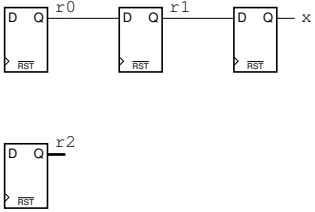

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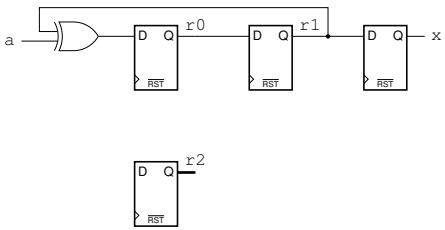

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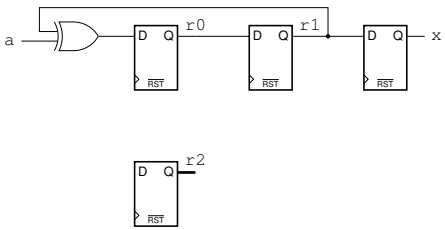

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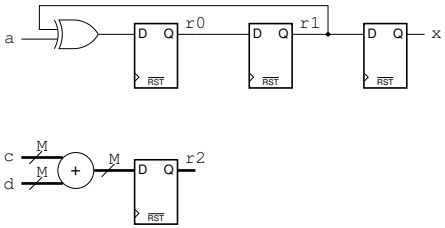

Example 2: Circuit - Combinational Process


```
19   process(all)
20     variable temp : std_ulogic;
21   begin
22     temp := '0';
23     for i in b'range loop
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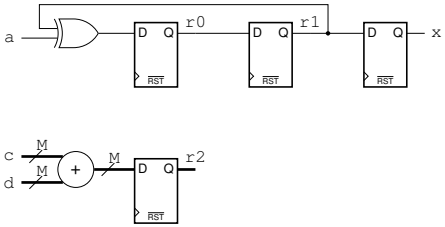

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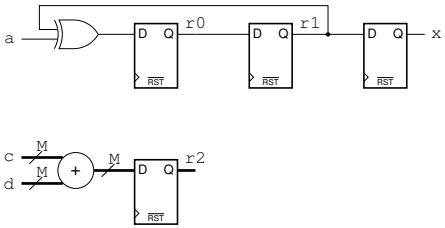

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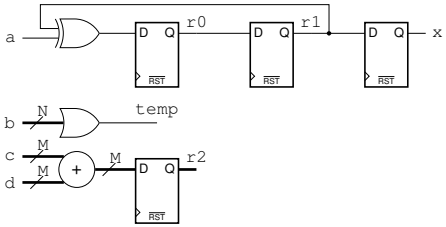

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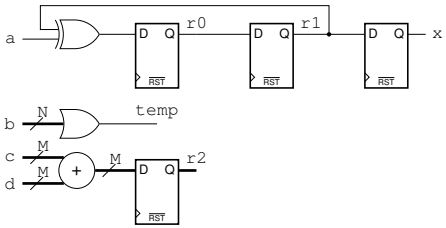

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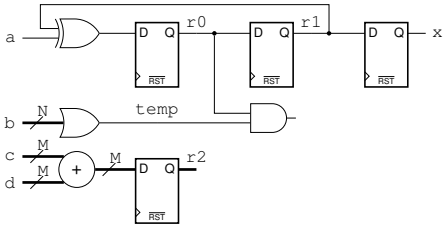

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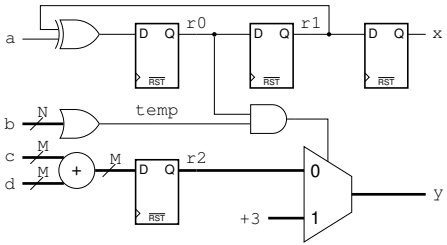

Lecture Complete!