Hardware Modeling [VU] (191.011)
– WS25 –
Behavioral Modeling

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WS 2025/26

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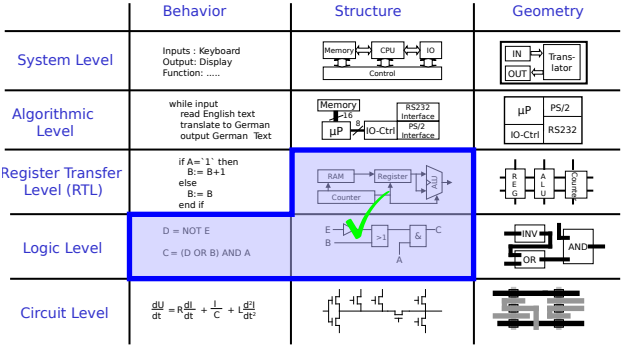
Introduction

- Concurrent assignments and structural modeling
  - Can model all **combinational** hardware
  - Hardly scales...



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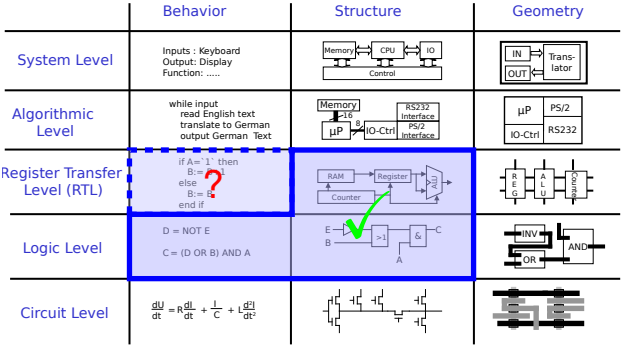

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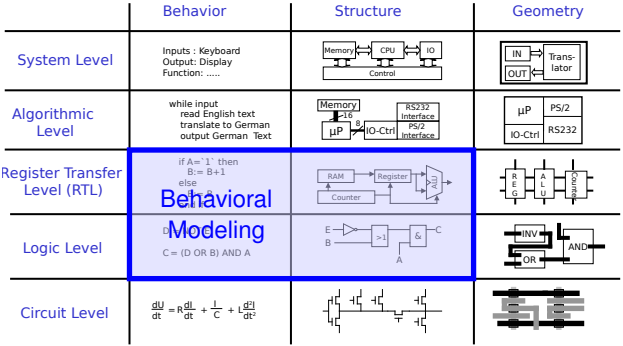

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- **Complements** struct. modeling and concurrent assignments
- Ubiquitous in synchronous designs

Example: Multiplexer


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5    port (
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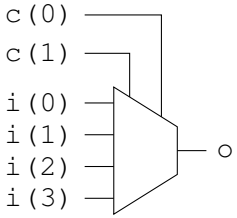

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15        i(1) when not c(1) and     c(0) else
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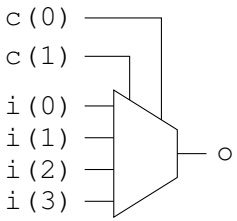

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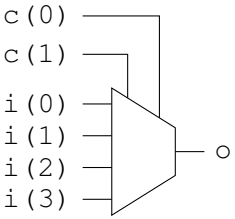

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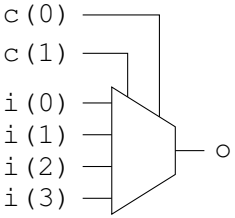

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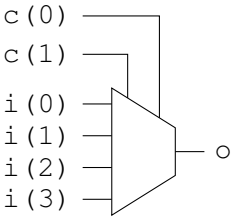

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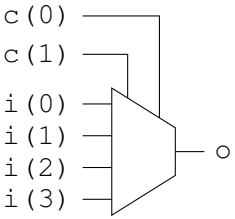
⇒ “Termination” of circuit?!



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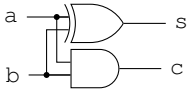

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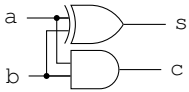


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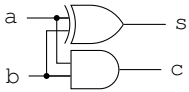


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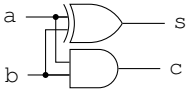


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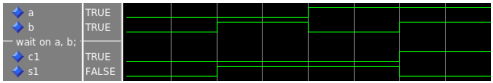

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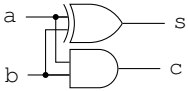


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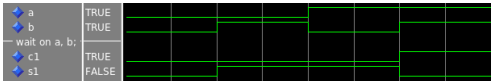

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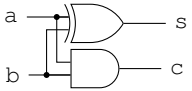


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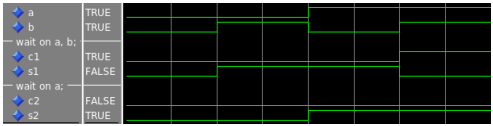

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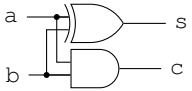


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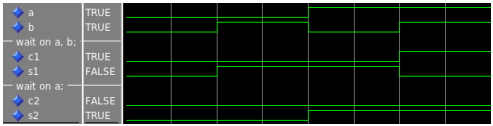

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⇒ `all` keyword for sensitivity lists

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- Rule of thumb: Use `all` for comb. processes

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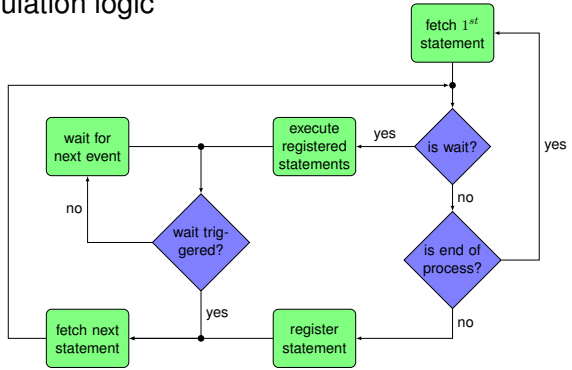
$\Rightarrow$ Process simulation logic



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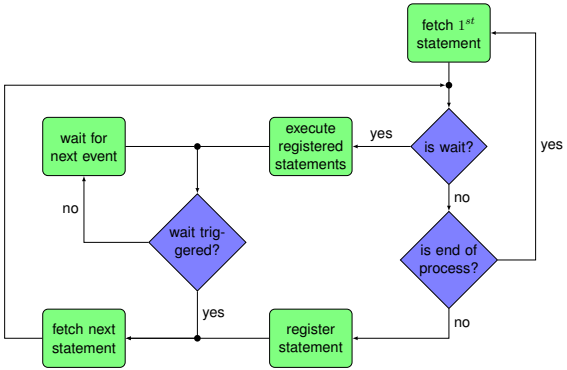

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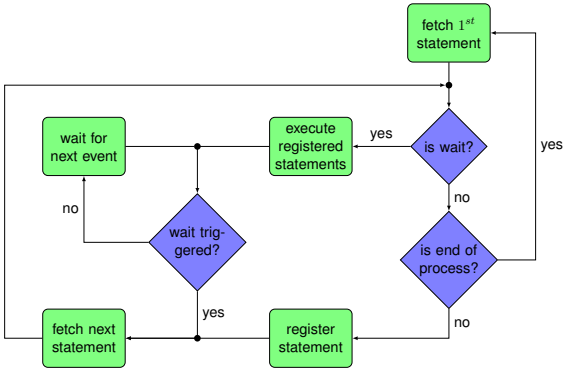
7      c <= b;
8      wait on a, b;
9    end process;
10 end architecture;
```

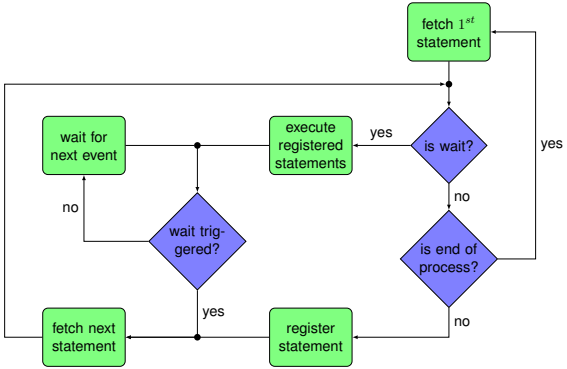


a: false
b: false
c: false

Example: Process Simulation

Input `a` changes

```
1  architecture beh of abc is
2    signal a, b, c : boolean;
3  begin
4    process
5    begin
6      b <= a;
7      c <= b;
8      wait on a, b;
9    end process;
10 end architecture;
```

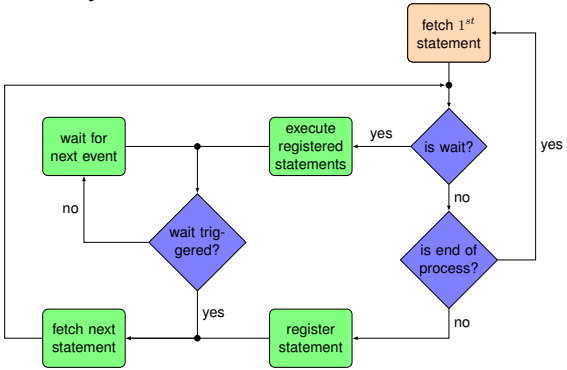


a: `false` → `true`
b: `false`
c: `false`

Example: Process Simulation

Fetch first statement of the process body

```
1  architecture beh of abc is
2    signal a, b, c : boolean;
3  begin
4    process
5    begin
6      b <= a;
7      c <= b;
8      wait on a, b;
9    end process;
10 end architecture;
```

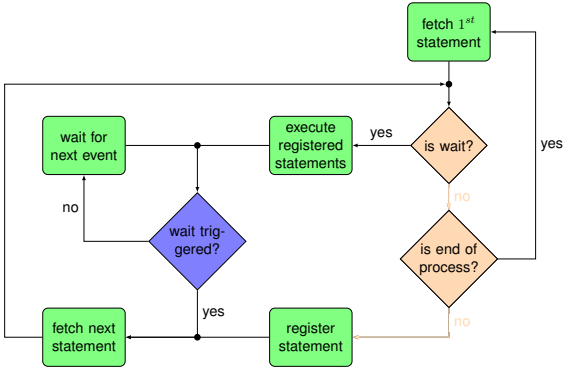


a: `true`
b: `false`
c: `false`

Example: Process Simulation

Neither `wait` nor `end process`

```
1  architecture beh of abc is
2    signal a, b, c : boolean;
3  begin
4    process
5    begin
6      b <= a;
7      c <= b;
8      wait on a, b;
9    end process;
10 end architecture;
```

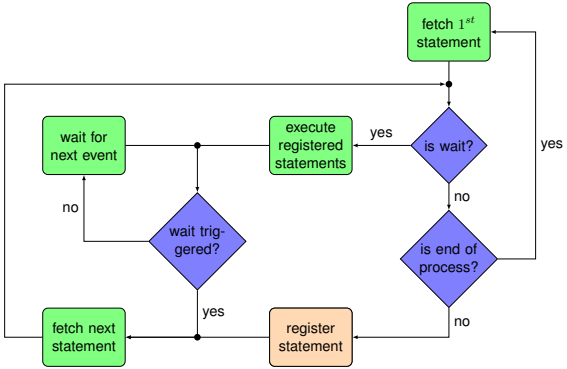


a: `true`
b: `false`
c: `false`

Example: Process Simulation

Register statement for **future** execution

```
1  architecture beh of abc is
2    signal a, b, c : boolean;
3  begin
4    process
5    begin
6      b <= a;
7      c <= b;
8      wait on a, b;
9    end process;
10 end architecture;
```



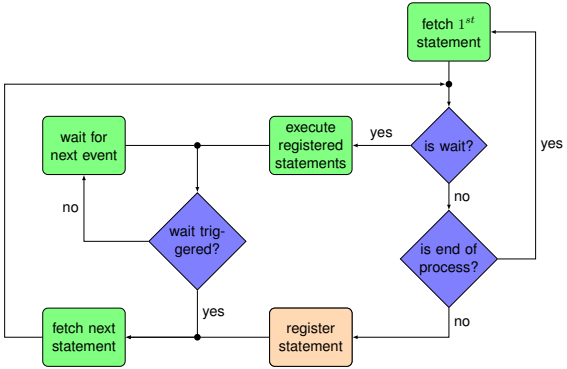
a: `true`
b: `false`
c: `false`

Registered: `b <= true;`

Example: Process Simulation

Register statement for **future** execution

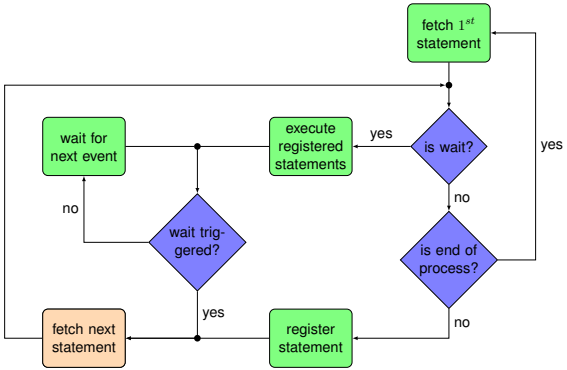
```
1  architecture beh of abc is
2    signal a, b, c : boolean;
3  begin
4    process
5    begin
6      b <= a;
7      c <= b;
8      wait on a, b;
9    end process;
10 end architecture;
```



Example: Process Simulation

Fetch the next statement

```
1  architecture beh of abc is
2    signal a, b, c : boolean;
3  begin
4    process
5    begin
6      b <= a;
7      c <= b;
8      wait on a, b;
9    end process;
10 end architecture;
```



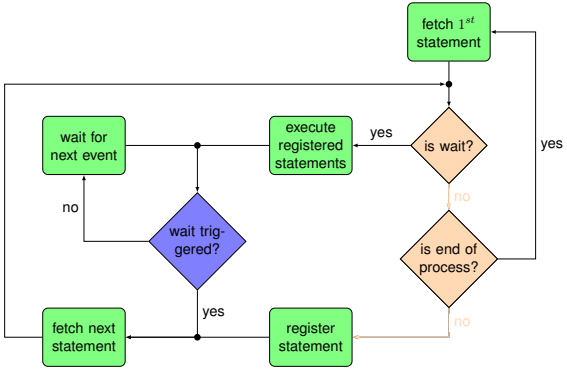
a: `true`
b: `false`
c: `false`

Registered: `b <= true;`

Example: Process Simulation

Continue until `wait` nor `end process` encountered

```
1  architecture beh of abc is
2    signal a, b, c : boolean;
3  begin
4    process
5    begin
6      b <= a;
7      c <= b;
8      wait on a, b;
9    end process;
10 end architecture;
```



a: `true`
b: `false`
c: `false`

Registered: `b <= true;`

Example: Process Simulation

Continue until `wait` nor `end process` encountered

```
1  architecture beh of abc is
2    signal a, b, c : boolean;
3  begin
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5    begin
6      b <= a;
7      c <= b;
8      wait on a, b;
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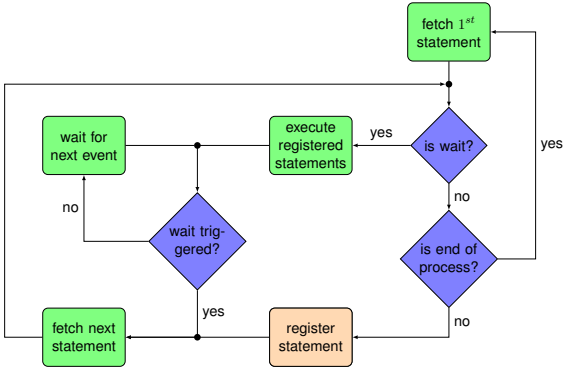
10 end architecture;
```



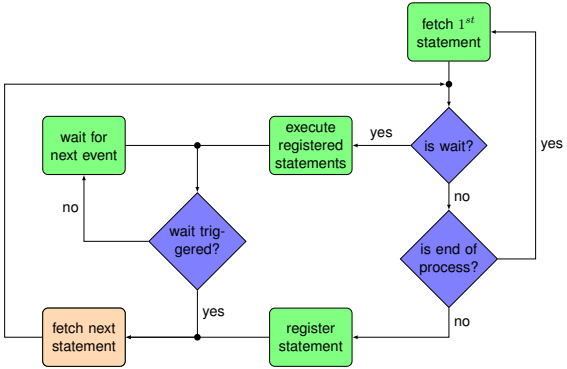
a: `true`
b: `false`
c: `false`

Registered: `b <= true;`
`c <= false;`

Example: Process Simulation

Continue until `wait` nor `end process` encountered

```
1  architecture beh of abc is
2    signal a, b, c : boolean;
3  begin
4    process
5    begin
6      b <= a;
7      c <= b;
8      wait on a, b;
9    end process;
10 end architecture;
```



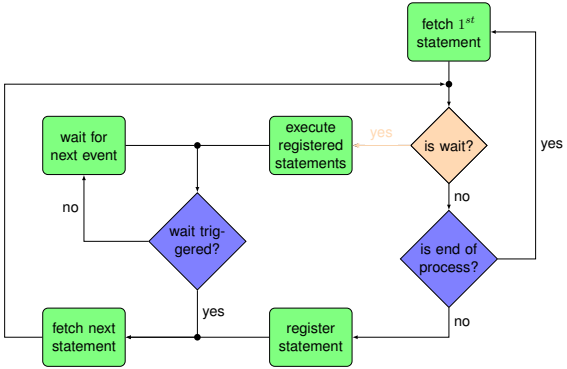
a: `true`
b: `false`
c: `false`

Registered: `b <= true;`
`c <= false;`

Example: Process Simulation

`wait` statement encountered

```
1  architecture beh of abc is
2    signal a, b, c : boolean;
3  begin
4    process
5    begin
6      b <= a;
7      c <= b;
8      wait on a, b;
9    end process;
10 end architecture;
```



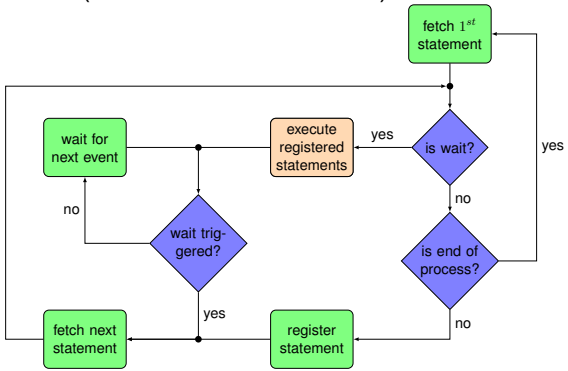
a: `true`
b: `false`
c: `false`

Registered: `b <= true;`
`c <= false;`

Example: Process Simulation

Now execute **all** registered statements (in zero simulation time)

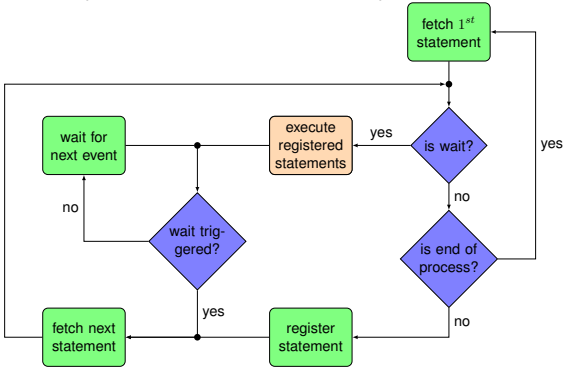
```
1  architecture beh of abc is
2    signal a, b, c : boolean;
3  begin
4    process
5    begin
6      b <= a;
7      c <= b;
8      wait on a, b;
9    end process;
10 end architecture;
```



Example: Process Simulation

Now execute **all** registered statements (in zero simulation time)

```
1  architecture beh of abc is
2    signal a, b, c : boolean;
3  begin
4    process
5    begin
6      b <= a;
7      c <= b;
8      wait on a, b;
9    end process;
10 end architecture;
```



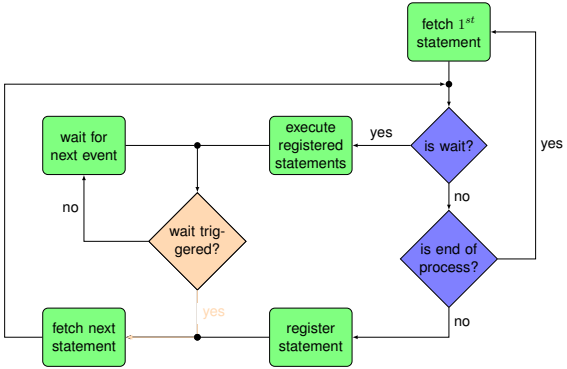
a: `true`
b: `true`
c: `false` → `false`

Registered: `c <= false;`

Example: Process Simulation

Change of `b` triggered `wait on a,b`

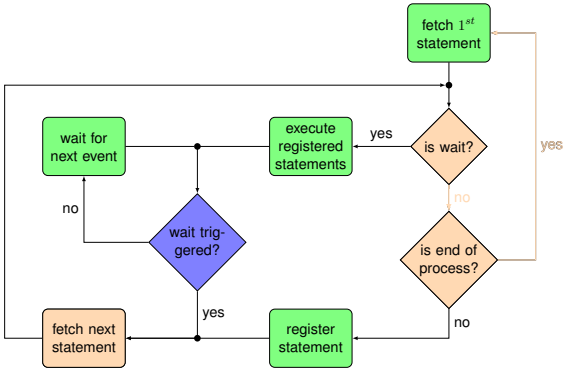
```
1  architecture beh of abc is
2    signal a, b, c : boolean;
3  begin
4    process
5    begin
6      b <= a;
7      c <= b;
8      wait on a, b;
9    end process;
10 end architecture;
```



Example: Process Simulation

Fetch next statement

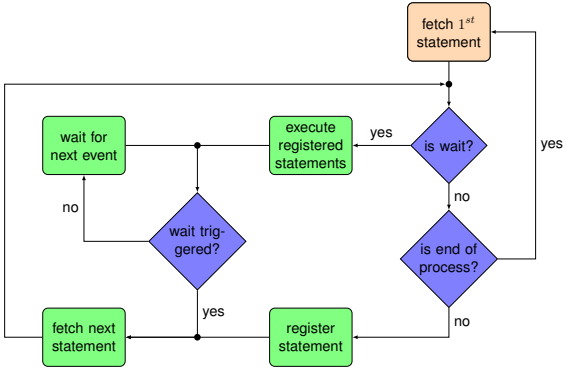
```
1  architecture beh of abc is
2    signal a, b, c : boolean;
3  begin
4    process
5    begin
6      b <= a;
7      c <= b;
8      wait on a, b;
9    end process;
10 end architecture;
```



Example: Process Simulation

End of process ⇒ Repeat

```
1  architecture beh of abc is
2    signal a, b, c : boolean;
3  begin
4    process
5    begin
6      b <= a;
7      c <= b;
8      wait on a, b;
9    end process;
10 end architecture;
```



a: `true`
b: `true`
c: `false`

Registered:

Observations: Process Simulation

Observation I

Statements are not executed immediately, but rather gathered until a wait is encountered. Then they are all executed without consuming simulation time. This mimics a concurrent execution.

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Without `b` in the sensitivity list in the example, `c` would end remaining `false` until the next change of `a` $\Rightarrow$ proper sensitivity list paramount.

Observations: Process Simulation

Observation I

Statements are not executed immediately, but rather gathered until a wait is encountered. Then they are all executed without consuming simulation time. This mimics a concurrent execution.

Observation II

Without `b` in the sensitivity list in the example, `c` would end remaining `false` until the next change of `a` $\Rightarrow$ proper sensitivity list paramount.

Observation III

A process without (implicit) `wait` statement loops endlessly.

Variables

- Signal assignments executed at `wait`

Variables

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$\Rightarrow$ Variables

Variables

- Signal assignments executed at `wait`

$\Rightarrow$ Variables

  - In process declarative part

```
variable x : integer := 10;
```

Variables

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⇒ Variables

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variable x : integer := 10;
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- **Not** in sensitivity list

Variables

- Signal assignments executed at `wait`

⇒ Variables

- In process declarative part

```
variable x : integer := 10;
```

- Assignments (`:=`) have *immediate* effect
- **Not** in sensitivity list
- Name and reuse intermediate expressions

Variables

- Signal assignments executed at `wait`

⇒ Variables

  - In process declarative part
    ```
    variable x : integer := 10;
    ```
  - Assignments (`:=`) have *immediate* effect
  - **Not** in sensitivity list
  - Name and reuse intermediate expressions

- Example

```
1  entity wide_and is
2  port(
3   i : in std_ulogic_vector;
4   o : out std_ulogic
5  );
```

```
1  process (all) is
2   variable result : std_ulogic := '1';
3  begin
4   for x in i'range loop
5    result := result and i(x);
6   end loop;
7   o <= result;
8  end process;
```

Variables

- Signal assignments executed at `wait`

⇒ Variables
  - In process declarative part
    `variable x : integer := 10;`
  - Assignments (`:=`) have *immediate* effect
  - **Not** in sensitivity list
  - Name and reuse intermediate expressions

- Example

```
1  entity wide_and is
2  port(
3   i : in std_ulogic_vector;
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```
1  process (all) is
2   variable result : std_ulogic := '1';
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```

Example: Variables vs Signals

Example: Variables vs Signals


```
1  architecture sig of app is
2    signal w, x, y, z : std_ulogic;
3  begin
4    process (all) begin
5      x <= a;
6      y <= b;
7      z <= x and y;
8      y <= c;
9      w <= x and y;
10   end process;
11 end architecture;
```

Example: Variables vs Signals

```
1  architecture sig of app is
2    signal w, x, y, z : std_ulogic;
3  begin
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```

Initial Values: `A=B=C=W=X=Y=Z='1', C='1'→'0'`

Example: Variables vs Signals


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1  architecture sig of app is
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```

Initial Values: `A=B=C=W=X=Y=Z='1', C='1'→'0'`

Iteration #	signal values at end
1	`x='1'`
2	

Example: Variables vs Signals


```
1  architecture sig of app is
2    signal w, x, y, z : std_ulogic;
3  begin
4    process (all) begin
5      x <= a;
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Initial Values: `A=B=C=W=X=Y=Z='1', C='1'→'0'`

Iteration #	signal values at end
1	`x='1', y='1'`
2	

Example: Variables vs Signals

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1  architecture sig of app is
2    signal w, x, y, z : std_ulogic;
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Initial Values: `A=B=C=W=X=Y=Z='1', C='1'→'0'`

Iteration #	signal values at end
1	x='1', y='1' z='1'
2	

Example: Variables vs Signals


```
1  architecture sig of app is
2    signal w, x, y, z : std_ulogic;
3  begin
4    process (all) begin
5      x <= a;
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7      z <= x and y;
8      y <= c;
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Iteration #	signal values at end
1	x='1', y='0' z='1'
2	

Example: Variables vs Signals


```
1  architecture sig of app is
2    signal w, x, y, z : std_ulogic;
3  begin
4    process (all) begin
5      x <= a;
6      y <= b;
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Iteration #	signal values at end
1	`x='1', y='0'` `z='1', w='1'`
2	

Example: Variables vs Signals


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1	`x='1', y='0'` `z='1', w='1'`
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Example: Variables vs Signals


```
1  architecture sig of app is
2    signal w, x, y, z : std_ulogic;
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9      w <= x and y;
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```

```
1  architecture var of app is
2    signal w, z : std_ulogic;
3  begin
4    process (all) is
5      variable x, y : std_ulogic;
6    begin
7      x := a;
8      y := b;
9      z <= x and y;
10     y := c;
11     w <= x and y;
12   end process;
13 end architecture;
```

Initial Values: `A=B=C=W=X=Y=Z='1', C='1'→'0'`

Iteration #	signal values at end
1	x='1', y='0' z='1', w='1'
2	w='0', x='1' y='0', z='0'

Example: Variables vs Signals


```
1  architecture sig of app is
2    signal w, x, y, z : std_ulogic;
3  begin
4    process (all) begin
5      x <= a;
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Initial Values: `A=B=C=W=X=Y=Z='1', C='1'→'0'`

Iteration #	signal values at end
1	`x='1', y='0'` `z='1', w='1'`
2	`w='0', x='1'` `y='0', z='0'`

Example: Variables vs Signals


```
1  architecture sig of app is
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Iteration #	signal values at end
1	`x='1', y='0'` `z='1', w='1'`
2	`w='0', x='1'` `y='0', z='0'`

Iteration #	signal values at end
1	
2	

Example: Variables vs Signals


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1  architecture sig of app is
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7      x := a;
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9      z <= x and y;
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```

Initial Values: `A=B=C=W=X=Y=Z='1', C='1'→'0'`

Iteration #	signal values at end
1	x='1', y='0' z='1', w='1'
2	w='0', x='1' y='0', z='0'

Iteration #	signal values at end
1	x='1', y='1'
2	

Example: Variables vs Signals


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1  architecture sig of app is
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3  begin
4    process (all) is
5      variable x, y : std_ulogic;
6    begin
7      x := a;
8      y := b;
9      z <= x and y;
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Iteration #	signal values at end
1	x='1', y='0' z='1', w='1'
2	w='0', x='1' y='0', z='0'

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2	

Example: Variables vs Signals


```
1  architecture sig of app is
2    signal w, x, y, z : std_ulogic;
3  begin
4    process (all) begin
5      x <= a;
6      y <= b;
7      z <= x and y;
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9      w <= x and y;
10   end process;
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1  architecture var of app is
2    signal w, z : std_ulogic;
3  begin
4    process (all) is
5      variable x, y : std_ulogic;
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Initial Values: `A=B=C=W=X=Y=Z='1', C='1'→'0'`

Iteration #	signal values at end
1	x='1', y='0' z='1', w='1'
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Example: Variables vs Signals


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Not the same circuit!

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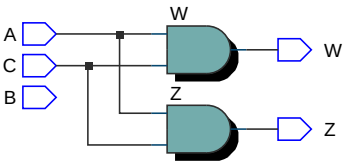
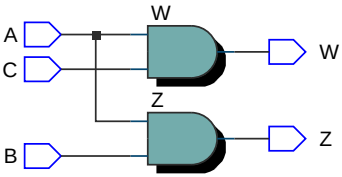
Variables vs Signals (Cont'd)

⇒ Use of `variable` and `signal` not equivalent!

Signals



Variables



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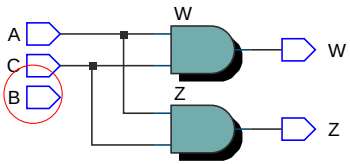

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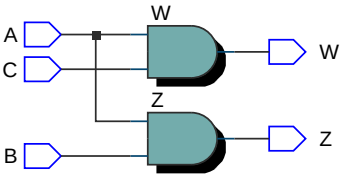

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  - Executed concurrently
  - Order of actual execution *undefined* $\Rightarrow$ do not rely on it

Lecture Complete!